Variable Length Optical Packet Synchronizer

John P. Mack, Henrik N. Poulsen, and Daniel J. Blumenthal, *Fellow, IEEE*

***Abstract*—Synchronization of asynchronously arriving variable length Internet Protocol packets to a local clock is demonstrated using a fiber-based optical synchronizer. The synchronizer is a four-stage feed-forward design with a resolution of 853 ps and a dynamic tuning range of 12.8 ns. The arrival time of packets is determined on a per packet basis using a payload envelope detection technique. The synchronizer state is dynamically configured on a per packet basis determined from the arrival time. Layer-1 (bit-error-rate) measurements are presented with power penalties $<$0.5 dB and an input power dynamic range $>$15 dB. Layer-2 (packet recovery) measurements are presented with power penalties $<$1.5 dB.**

***Index Terms*—Optical switches, packet switching, semiconductor optical amplifiers (SOAs), synchronization.**

I. Introduction

OPTICAL packet switching (OPS) is a potential solution to achieving high-capacity routing while addressing the impending power and footprint limitations of ever increasing capacity electronic packet routing systems [1]. Packet-based networks scale well due to their asynchronous nature [2]. In today's networks, routers must be able to route variable length packets, ranging from 40 to 1500 bytes and possibly larger [3]. A major challenge in implementing OPS is to handle asynchronous arrival of packets at multiple input ports at each node to support functions such as optical buffering and forwarding [4]–[6].

In previously reported work, optical synchronization was demonstrated for fixed length packets ranging from 40 to 1120 bytes at a bit rate of 40 Gb/s or less [7]–[9]. These demonstrations utilized wavelength conversion or semiconductor optical amplifier (SOA)-based switches. The former reduces the number of active components required while the latter is more compact and amenable to integration. Synchronization of fixed length 48 byte packets using cascaded 1×2 integrated switches with fiber delay lines has been demonstrated at 2.5 Gb/s [10]. Choosing a synchronizer design that can be integrated is important for the scalability of optical packet switched routers.

In this work, we show for the first time optical synchronization of asynchronously arriving variable length 40-Gb/s packets. Dynamic synchronization on a per packet basis is demonstrated where the required delay is determined from an asynchronously arriving packet stream. The design we utilize can be integrated using an InP switch matrix butt coupled to silica-on-silicon waveguide delay lines as previously demonstrated for optical buffers [11].

Manuscript received March 26, 2008; revised April 25, 2008. This work was supported by the Defense Advanced Research Projects Agency (DARPA)/MTO and ARL under LASOR award W911NF-04-9-0001.

The authors are with the Electrical and Computer Engineering Department, University of California, Santa Barbara, CA 93106 USA (e-mail: jmack@ece.ucsb.edu).

Digital Object Identifier 10.1109/LPT.2008.926017

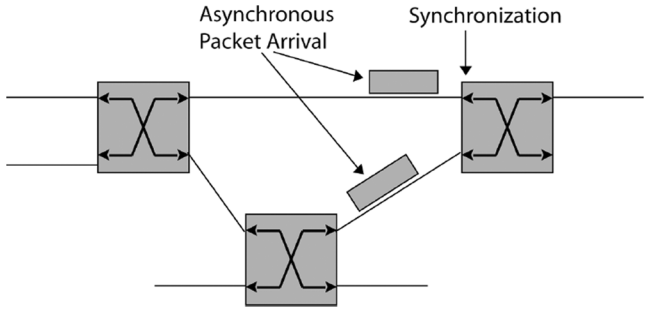

Fig. 1. Packets arrive asynchronously to optical switches.

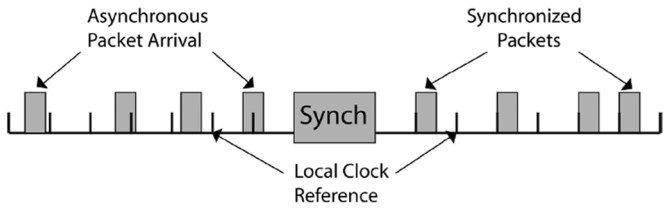

Fig. 2. Synchronization aligns asynchronous packets to a local clock.

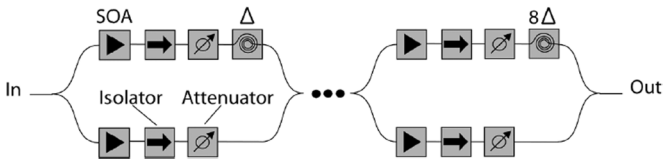

Fig. 3. Fiber-based four-stage synchronizer with SOA gates.

II. Synchronizer Design

The basic problem of asynchronous packet arrival is shown in Fig. 1. Packets arrive asynchronously to each node due to asynchronous operation and internode path length differences. In order to buffer and forward packets with high output link utilization, incoming packets must be synchronized to a local clock as shown in Fig. 2.

The synchronizer reported here is based on a feed-forward design that utilizes SOAs and fiber delay lines as illustrated in Fig. 3. While the demonstrated synchronizer was constructed using discrete components, it is amenable to implementation using integrated switches and delays. SOAs were used as the gates to select the required delay and compensate for losses. In order to suppress accumulated amplified spontaneous emission, a bandpass filter with a bandwidth of 2.4 nm was placed at the output of the synchronizer. Attenuators were used to match path insertion losses, yielding an average and standard deviation of 3.43 and 0.22 dB, respectively. The current injected into the

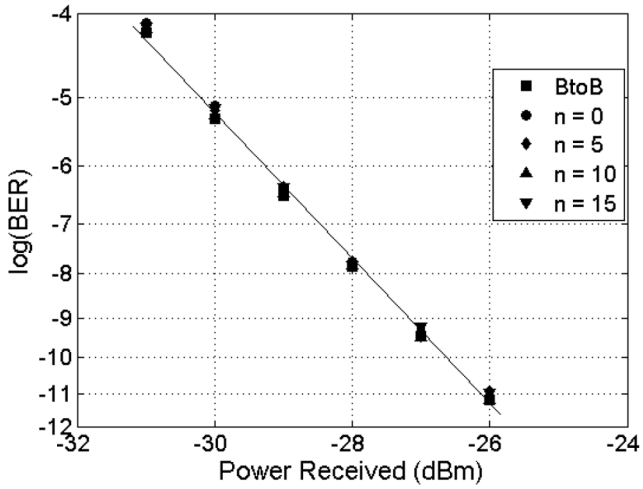

Fig. 4. Layer-1 (BER) measurements at input power $= -7$ dBm for synchronizer delays of $n = 0, 5, 10,$ and 15.

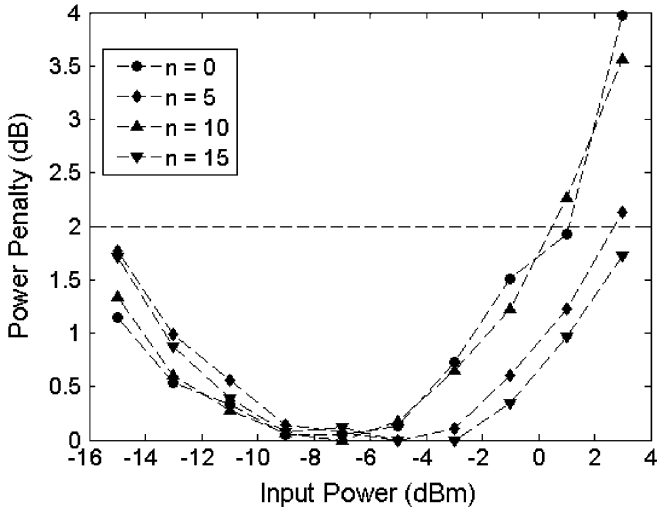

Fig. 5. Input power dynamic range measurements for synchronizer delays of $n = 0, 5, 10,$ and 15.

SOAs can be tuned to balance insertion losses and remove the need for attenuators.

The synchronizer temporal tuning range was chosen to match a local clock running at 78.125 MHz (12.8 ns). The local clock period was chosen to be slightly larger than the smallest packet size which is 40 bytes (8 ns). A four-stage synchronizer was used to provide a small enough resolution to compensate for the rise and fall times of an SOA-based switch. The relative delay through any configuration of the synchronizer can be given as $T(n) = n \times \Delta\ (n = 0, 1, 2 \ldots 15)$, where $\Delta = 853$ ps and the tuning range is 12.8 ns.

III. Static Performance Measurements

Layer-1 bit-error-rate (BER) measurements were conducted for a range of input powers into the synchronizer using pseudo-random bit sequence (PRBS) $2^{31}-1$ return-to-zero (RZ) data at 40 Gb/s under all possible static configurations. Fig. 4 shows BER plots at -7-dBm input power into the synchronizer for static settings of $n = 0, 5, 10,$ and 15. The power penalty is less than 0.5 dB for this input power. We conclude that neither SOA noise nor saturation limits performance for this set of operating conditions. The dynamic range is defined as the range of optical input powers into the synchronizer that yields error-free performance (10^{-9}) at less than 2-dB power penalty for a preamplified receiver as shown in Fig. 5. Input powers less than -9 dBm resulted in an increase in power penalty due to a degraded optical signal-to-noise ratio (OSNR). As the power is increased, the power penalty reaches a minimum. For high input powers greater than -5 dBm, saturation distorts the signal as well as decreases the gain of the SOAs which results in an increased power penalty due to patterning effects. The offset in the dynamic range curves can be attributed to a misbalance of gain and loss for the different paths. A dynamic range >15 dB was achieved for the various delays of the synchronizer.

IV. Dynamic Performance Measurements

Dynamic synchronizer operation with variable length packets is depicted in Fig. 6. An Internet traffic mixture, IMIX (7 : 4 : 1 ratio), stream consisting of 40-, 570-, and 1500-byte

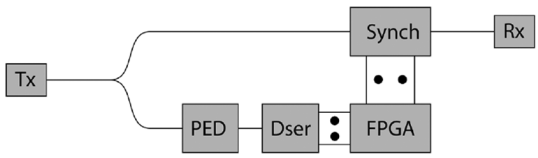

Fig. 6. Experimental setup of dynamic synchronization.

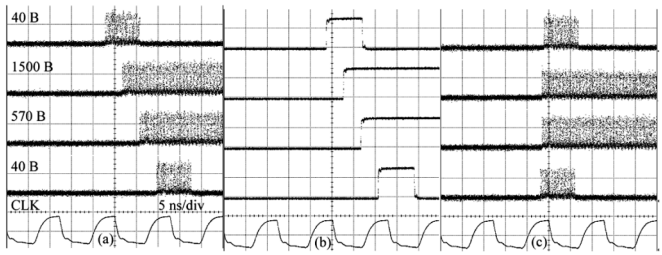

Fig. 7. (a) Asynchronous packets. (b) Recovered payload envelopes. (c) Synchronized packets.

RZ packets at 40 Gb/s were used which represents the most common packet lengths in current internet networks. Each packet consists of a 32-bit idler, 64-bit identifier, 8-bit header, and repeated PRBS 2^5-1. The data stream was engineered to test all possible states of the synchronizer. The data stream consists of 24 packets where each packet arrives relative to the local clock by $T(n) = n \times \Delta(n = 0, 1, 2, \ldots, 23)$ and the total period equals 4.5056 μs. Packets with $n = 0, 21, 10,$ and 15 and the 78.125-MHz local clock are depicted in Fig. 7(a). The relative skew between the local clock and the transmitted packets can be seen.

At the synchronizer input, a portion of the power is tapped and detected for payload envelope detection (PED). The PED is used to detect incoming asynchronous packets and generate packet envelopes as can be seen in Fig. 7(b). The PED consists of a 10-GHz photodetector followed by a 2.5-GHz limiting amplifier. The PED output enters a 1 : 16 deserializer (Dser) board operating at 10 GHz that allows the rising and falling edges of the packets to be sampled with a 100-ps resolution. The deserialized

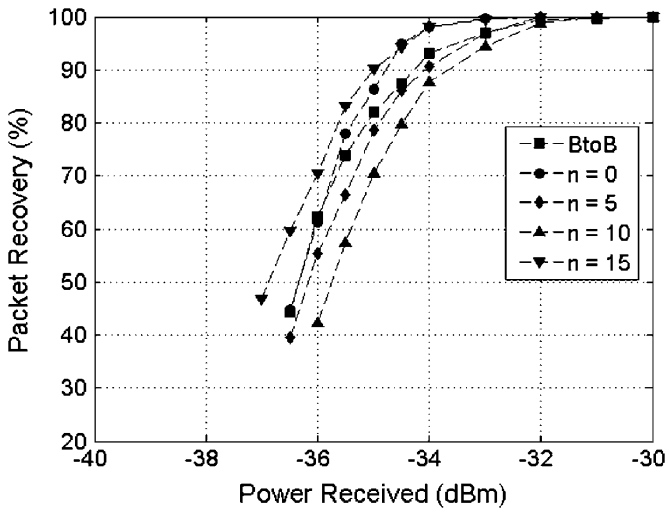

Fig. 8. Packet recovery measurements at input power $= -11.5$ dBm for synchronizer delays $n = 0, 5, 10,$ and 15.

envelope enters a field-programmable gate array (FPGA)-based board where it is further deserialized from 16 : 128 channels so that it can be processed in parallel by the 78.125-MHz local clock. In this experiment, the 10-GHz and 78.125-MHz clocks were derived from the transmitter to avoid the use of high-speed clock recovery circuits which would be necessary if the electronic control and transmitter were operated asynchronously. Here 16 channels of the deserialized envelopes are used which correspond to the delays of the synchronizer. The deserialized PED edges are compared to the rising edge of the local clock to determine the delay needed to synchronize incoming packets as well as the packet length. The FPGA generates SOA control signals that correspond to the required set of delays. If no envelope is detected then the FPGA turns off all SOAs in the synchronizer. SOA control signals are latched through D flip flops in order to match the total delay of each stage of the synchronizer and subsequently fed into voltage to current converters that drive the SOAs. Synchronization of packets to the local clock within 853 ps is shown in Fig. 7(c).

Layer-2 (packet recovery) performance was measured under dynamic tuning conditions for delays of $n = 0, 5, 10,$ and 15. Error-free performance was achieved for all packets with less than 1.5-dB power penalty as shown in Fig. 8. The variation in performance of the measured packets was caused by the difference in insertion losses for the various paths of the synchronizer. Since all packets arrive at the preamplified receiver in the same stream, the variation of insertion losses affect each packet's performance. Packets with lower insertion losses have a larger OSNR compared with those with high insertion losses. The difference in performance can be mitigated by reducing the variation of insertion losses.

V. Conclusion

This letter reports on the first implementation of a variable length optical packet synchronizer at 40 Gb/s. The synchronizer consisted of SOA-based switches with fiber delays. Layer-1 (BER) measurements were conducted with power penalties <0.5 dB and input power dynamic ranges >15 dB for several synchronizer delays. Autonomous synchronization was demonstrated using a PED, deserializer, and FPGA-based board for electronic control. The synchronizer dynamically aligned asynchronously arriving packets to a local clock with a resolution of 853 ps and tuning range of 12.8 ns. Layer-2 (packet recovery) measurements demonstrated error-free performance with power penalties <1.5 dB.

Further improvement of footprint, latency, and timing uncertainties can be achieved through the utilization of integrated technology. Footprint can be reduced through the use of integrated switches and waveguides. Latency of the switches used in the fiber-based synchronizer can be reduced from hundreds of nanoseconds to tens of picoseconds by using integrated switches. Finally, integrated waveguide technology can reduce the timing uncertainties which fiber-based delays can be constructed from hundreds of picoseconds to less than a picosecond. Therefore, integration will improve the scalability of synchronizers in optical switches.

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