INTEGRATION TECHNOLOGIES FOR AN 8X8 INP-BASED MONOLITHIC TUNABLE OPTICAL ROUTER WITH 40GB/S LINE RATE PER PORT

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Abstract

Large-scale photonic integration depends on robust epitaxial design and fabrication techniques. This paper reviews the integration strategy we developed to demonstrate an 8x8 InP-based monolithic tunable optical router capable of 40 Gbps operation per port.

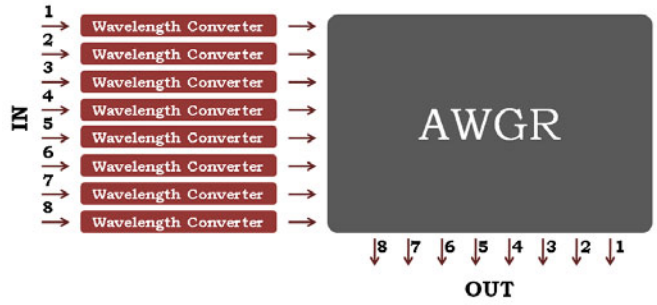
I. Introduction

Large-scale photonic integrated circuits (LS-PICs) in InP are a critical technology to manage the increasing bandwidth demands of next-generation optical networks. By integrating many of the network functions typically handled by discrete optical components into a single device, the overall system footprint can be appreciably reduced. Additionally, a compact, single-chip solution can provide performance and reliability gains along with a reduction in packaging costs. Although the promises of large-scale integration have long been known, LS-PICs have only recently emerged in the marketplace, thanks to advances in InP epitaxial growth and device fabrication that have led to improved yield [1,2].

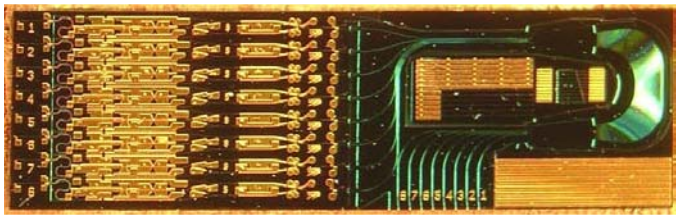
For most optical network applications, multi-channel LS-PICs that incorporate both active and passive device components on the same chip are desirable. Active/passive integration depends heavily on the epitaxial and fabrication schemes used. To this end, a number of different platform technologies have been proposed and developed in the last two decades [3-5]. Because the choice of an integration platform typically depends on the device requirements, there is not a one-size fits all integration solution. However, in general, an integration strategy should be designed to limit the degree of fabrication complexity and the number of epitaxial regrowth steps to provide high yield and lower cost.

All-optical packet switching at 40 Gbps is one application of interest for LS-PICs. In this approach, routing of data packets is confined solely to the optical domain, potentially easing the increasing power consumption demands of electronic-based routers at high data rates. As part of the U.S. Defense Advanced Research Projects Agency and U.S. Army sponsored DOD-N LASOR project [6], many important single-channel PIC building blocks such as wavelength converters, optical buffers and mode-locked lasers have been demonstrated [7]. Recently, we have further advanced our integration technologies to demonstrate multi-channel PICs with even greater component densities and chip functionality.

This paper will review the integration strategy we used to demonstrate an 8x8 monolithic tunable optical router (MOTOR) chip that serves as the packet-forwarding engine of an all-optical packet-switched router (Fig 1). The 8-channel device consists of an array of 8 tunable wavelength converters (WCs) and an arrayed-waveguide grating router (AWGR). It combines more than 200 building blocks into one chip and has a potential total data capacity of 640 Gbps. Single-channel operation of the device at 10 Gbps [8] and 40 Gbps [9,10] line rates has been achieved with reasonable power penalties. Our integration approach is based on quantum-well intermixing (QWI) and leverages risk by using only a single blanket epitaxial regrowth. To provide additional component functionality, advanced InP fabrication techniques are used to define three separate waveguide architectures that provide differing levels of optical confinement.



(a)



(b)

Fig. 1. a) Schematic of MOTOR chip architecture; (b) Photograph of fabricated 8-channel device

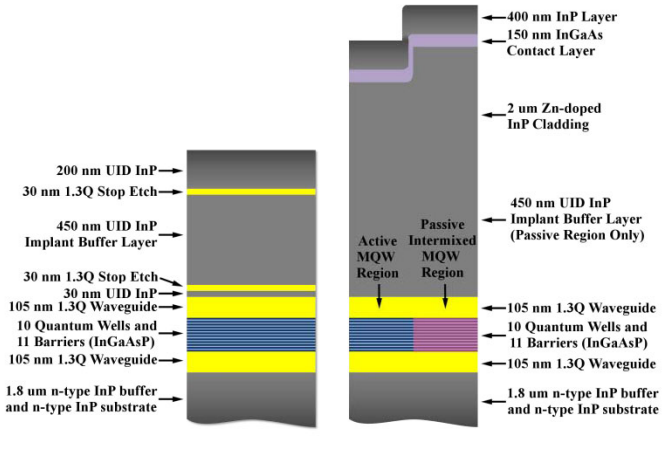
II. Device Design

Our integration strategy for the MOTOR chip was largely based on the design requirements of the WCs and AWGR. Wavelength conversion is accomplished through the use nonlinear semiconductor optical amplifiers (SOA) within a Mach-Zehnder interferometer (MZI) as in [11]. Input data pulses to these SOAs can cause a phase shift in the MZI to modulate an input CW signal, provided that the SOAs are sufficiently saturated. These SOAs necessarily require a high degree of optical confinement. In contrast to these saturated SOAs, the device also needs linear SOAs to amplify the input data signal before the MZI. Therefore, our integration approach must allow for the realization of both linear and nonlinear SOAs. To overcome the inherent limitations of slow carrier recovery time between input data pulses in the MZI SOA, each WC must also employ an integrated delay line to time-delay input pulses to one branch of the MZI relative to the other. Lastly, the WCs require integration of low-loss passive waveguides, splitters and phase tuners.

The AWGR at the output of the WCs should have a small footprint (which constrains the channel spacing), low insertion loss and low propagation loss. The loss is mainly governed by proper design of the input and output star coupler region and the waveguide fabrication. Most notably, the etch process used should provide smooth sidewalls in order to minimize scatter loss and good uniformity across the AWGR section to minimize index variations.

III. Integration Strategy

To achieve the functionality required for the MOTOR chip, we developed a four-point integration strategy. First, an epitaxial base structure in which the multiple quantum well (MQW) active region is sandwiched in the center of the passive waveguide layers is used in order to maximize optical confinement. This ensures that we can obtain the nonlinear MZI SOAs that are essential to wavelength conversion. Linear SOAs can also be realized with this approach, but their length must be kept short to prevent saturation. However, this limits the total possible gain. Second, QWI is employed to blue-shift the active band edge from an as-grown PL wavelength of 1545 nm to a passive band edge of 1420 nm. This allows us to achieve low propagation loss and efficient phase tuners (due to the presence of detuned MQWs in the passive sections). Third, a single blanket p-type InP regrowth is used to clad the waveguide. Blanket regrowths have the advantage of simplicity and higher yield. However, using only one p-doped regrowth step can lead to increased propagation losses in passive regions. The technique we developed to address this issue is discussed in the next section. Finally, our device utilizes three different waveguide architectures so that components with differing optical confinement (and hence optical properties) can be realized. The specifics associated with these waveguide designs are also discussed below.



(a) (b)

Fig. 2. a) Base epitaxial structure; (b) Epitaxial structure after regrowth (the undoped buffer layer found in some passive regions of the device is also shown)

A. Passive Propagation Loss Reduction with Single Regrowth

It is well known that the interaction of an optical mode with Zn-doped InP can lead to significant loss via free-carrier absorption. In fact, this loss has been shown to be on the order of 20 cm^{-1} for every 1E18 cm^{-3} doping at a wavelength of 1.5 μm [12]. Doping of this level is required in active sections of our device to make efficient diodes. Since we limit our process to only one regrowth step, this means we would have equivalent doping in our passive sections and consequently high loss. This problem could be addressed through an additional undoped regrowth in passive regions, but that is not ideal in terms of cost and yield.

Our base growth (Fig. 2a) contains an undoped InP buffer layer above the MQW region. Historically, this layer has been used exclusively for QWI, after which it is selectively removed via wet etching [3]. However, there is no reason that this layer must be removed after QWI, so we now deliberately leave the buffer layer in certain passive regions of the chip (Fig. 2b) [13]. This effectively "inserts" an unintentionally doped (UID) setback layer between the optical mode and the Zn dopant atoms in the p-type cladding, thus reducing optical scattering losses. The key advantage with this approach is that no additional regrowth is required. Simulations have shown that the net loss with this approach can be decreased by as much as much as ~2.4X, depending on the waveguide structure.

B. Waveguide Designs and Implementation

The MOTOR chip can be divided into three sections with differing ideal optical requirements. To improve the performance of components in these regions, multiple waveguide architectures are defined across the device. First, the bulk of the WC array is defined with a surface ridge waveguide (Fig. 3a,c). This design is used primarily due to its fabrication simplicity and because it provides efficient pumping in gain regions. The waveguide is fabricated by both dry and wet chemical etching. A 400-nm PECVD SiO_2 hard mask is defined above the InP cladding by lithography and then CHF_3-based inductively-coupled plasma (ICP) dry

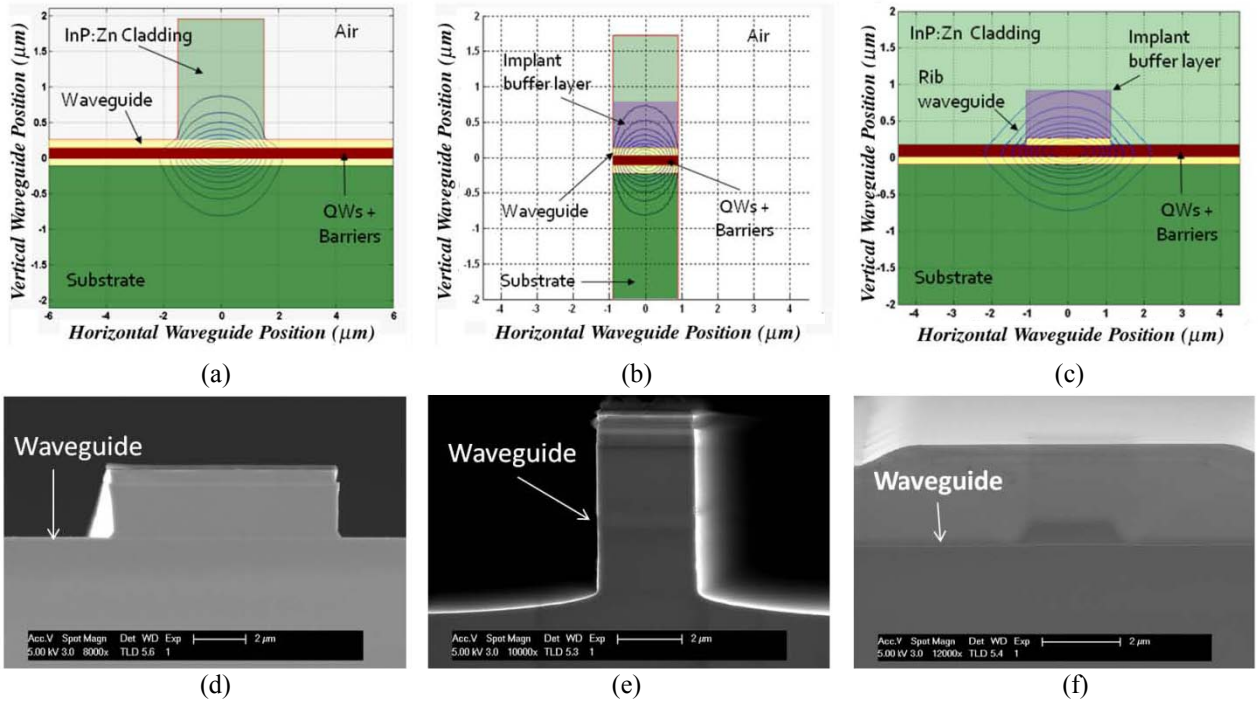


Fig 3. Waveguide architectures used in MOTOR: (a), (b), (c) show schematic cross-sections with the optical mode profile superimposed for surface ridge, deeply-etched ridge, and buried rib, respectively. (d), (e), (f) show SEM cross sections for surface ridge, deeply-etched ridge, and buried rib, respectively

etching. The InP ridge is etched via ICP to a depth of 1.8 μm in a Cl_2:H_2:Ar-based chemistry. By optimizing the gas flows and power levels, straight and smooth sidewalls can be obtained [14]. The remaining 0.6 μm of InP cladding is then removed by selective wet etching in a 3:1 H_3PO_4:HCl mixture. The quaternary waveguide layer above the MQW acts as a stop-etch layer. Because the etch does not go through the MQW region, we avoid surface recombination issues. However, the wet etch is crystallographic and the structure has relatively low lateral confinement, so high-angle structures and tight bends are problematic.

Second, to achieve the differential delay in the MZI that is required for 40 Gbps operation, a compact, 11-ps delay line is needed on chip. In order to minimize the footprint of this component, a deeply-etched waveguide structure is utilized (Fig 3b,e). The delay is fabricated using two dry etch steps. The first 1.8-μm etch is performed simultaneously with the dry-etch step of the surface ridge waveguide. Precise alignment between the surface ridge and deeply-etched regions is maintained because they share the same hard mask. The delay line region is protected with photoresist during the wet etch of the surface ridge. Next, a 350 nm PECVD SiO_2 hard mask is lifted off to open vias in the delay line region. A 2-3 μm dry etch that goes through the waveguide/MQW layers (using identical etch conditions as the first dry etch) is then performed. Since the deeply-etched waveguides are only used in passive sections, surface recombination is not relevant. However, because the optical mode can laterally interact with etched sidewalls, it is extremely important that the sidewalls are not rough.

The AWGR is defined with a 70-nm deep shallow rib waveguide that is etched into the upper waveguide layer (above the MQW) *prior* to the cladding regrowth, which subsequently buries it (Fig. 3c,f). Because a selective wet etch is avoided, this rib waveguide can be turned a full 180° to achieve a compact AWGR footprint. The insertion loss at the star couplers with this architecture is also low in comparison with that of a deeply-etched design.

IV. Results

The spectral response of the AWGR to amplified spontaneous emission (ASE) generated by forward biasing the MZI SOAs was measured in an optical spectrum analyzer. Fig. 4 shows the ASE spectrum from each output port using the SOAs in input port #3. The AWGR is well behaved with a free spectral range of 11.1 nm. Next, the wavelength-based switching capacity of the device was examined by biasing the SG-DBR of input port #3. Fig. 4 shows that with proper biasing of the mirror diodes, the wavelength of the laser can be tuned to the allowed wavelength of any output port. Output powers of more than -5 dBm were measured. This power level is reasonable given the long propagation length in the AWGR region and fiber coupling losses (~4-5 dB).

40 Gbps wavelength conversion and channel switching were then investigated by sending a modulated input data source into the chip and measuring the bit-error rate (BER) of the converted and routed data [10]. Fig. 5 shows that power penalties as low as 4.5 dB were achieved at a BER of $< 10^{-9}$ for multiple input/output port combinations.

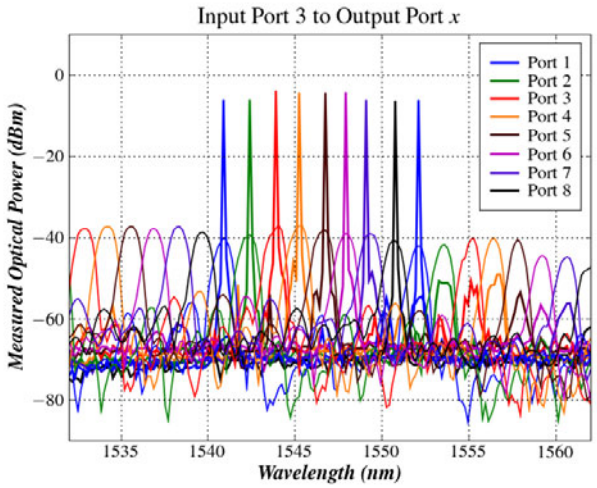


Fig. 4. ASE spectra from all output ports. Lasing spectra from the SG-DBR of input channel #3 (tuned with various mirror bias levels) from each output are superimposed to demonstrate the wavelength switching capacity of the device

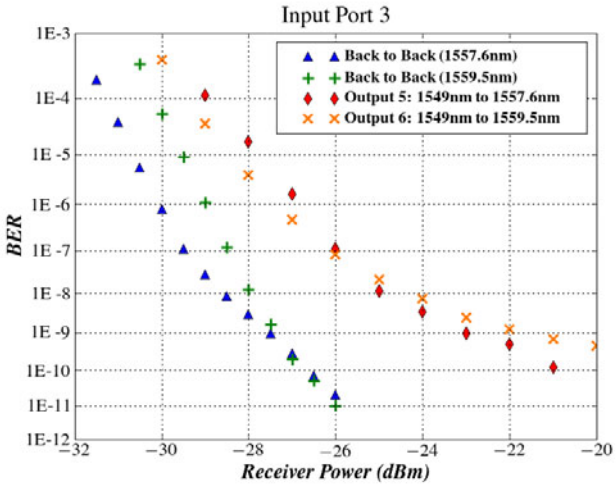


Fig. 5. BERs at 40 Gbps measured from a constant input port using multiple output ports

V. Conclusion

Using an integration strategy that emphasized simplicity for the sake of yield, we have demonstrated one of the most complex LS-PICs to date. Our strategy combines epitaxial techniques such as QWI and simple blanket regrowths with aggressive waveguide fabrication techniques. Notably, our device employed only one p-type InP regrowth step. Because the doping profile of the cladding region was designed for active components, steps were devised to reduce optical loss in passive regions. We now leave an InP implant buffer layer (used previously only for QWI) above the waveguide in passive regions to separate the optical mode from the p-type dopant in the cladding without additional regrowth steps. We have also demonstrated multiple waveguide architectures on a single-chip in order to optimize components with different optical properties. The execution of this integration strategy has led to a successful demonstration of single-channel wavelength conversion and routing of data at 40 Gbps.

Acknowledgements

This work was supported by the U.S. Defense Advanced Research Projects Agency's Microelectronics Technology Office and the U.S. Army under the DOD-N LASOR Project (W911NF-04-9-0001). Device fabrication was done in the UCSB nanofabrication facility, part of the U.S. National Science Foundation funded National Nanotechnology Infrastructure Network.

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