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# A PACKET-RATE REAL-TIME RECONFIGURABLE PHOTONIC SWITCH FOR COMPUTER INTERCONNECTS

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Multistage, multihop photonic interconnection networks with deflection routing can allow tightly coupled multiprocessor computers to scale to large number of processors over large physical areas [1]. Deflection routing handles the routing and contention functions and is well matched to flow-through photonic switches. A key component of these networks is the 2x2 photonic switch capable of self-routing packets and resolving contention for its output ports. A 2x2 photonic switch which performs deflection routing in real-time has been demonstrated [2]. The reported switch processes packets that are coded using bit per wavelength coding (BPW). An electronic EPROM lookup table was used to map all $2^6$ possible control bits from the two switch inputs to a single control signal. Switch throughput was on the order of 10 Mbit/s and latency on the order of 1 μs.

Two important features are scalability to large numbers of nodes and robustness to changing traffic and network conditions. The routing control processor (RCP) is responsible for computing the switch state, and should scale as the number of nodes increases. Additionally, if network conditions change, e.g. if a link goes down, the RCP should be able to adapt. Real-time reconfigurable switches offer the potential to adapt to changing conditions. optoelectronic based processors can be used to realize real-time reconfigurable architectures with low latency and the added benefit that they scale well with increasing network size.

In this paper we discuss a novel reconfigurable switch architecture and its demonstration with improved performance over the previously reported switch in terms of latency and flexibility. We also discuss the salient features which provides reconfiguration at the packet rate. Details of an optoelectronic processor which allows the control function to be changed dynamically will be discussed. Additionally, a method to extend this technique to react to slowly varying traffic conditions will also be presented.

## 1.0 Switch Architecture

The overall architecture is shown in Figure 1a. Packets are coded using BPW coding. Control bits centered about $\{\lambda_c\}$ are demultiplexed from data bits centered about $\{\lambda_d\}$. Data bits are stored in a fiber delay line equivalent to the processor latency. The control bits are further demultiplexed and directed to an optoelectronic RCP, where the priority and address bits are sent to separate stages. The RCP generates a control signal for the 2X2 switch. Contention occurs when both inputs request the same switch output port. *Deflection routing* [3] uses the priority bits to determine the switch state. Under a contention condition, the packet with the higher priority bit will route to its desired output while the other input is deflected. The deflected packet will reach its destination via an alternate path in the network topology [1]. In the case where contention exists and the priority bits are equal, the switch is maintained in its prior state to promote fairness.

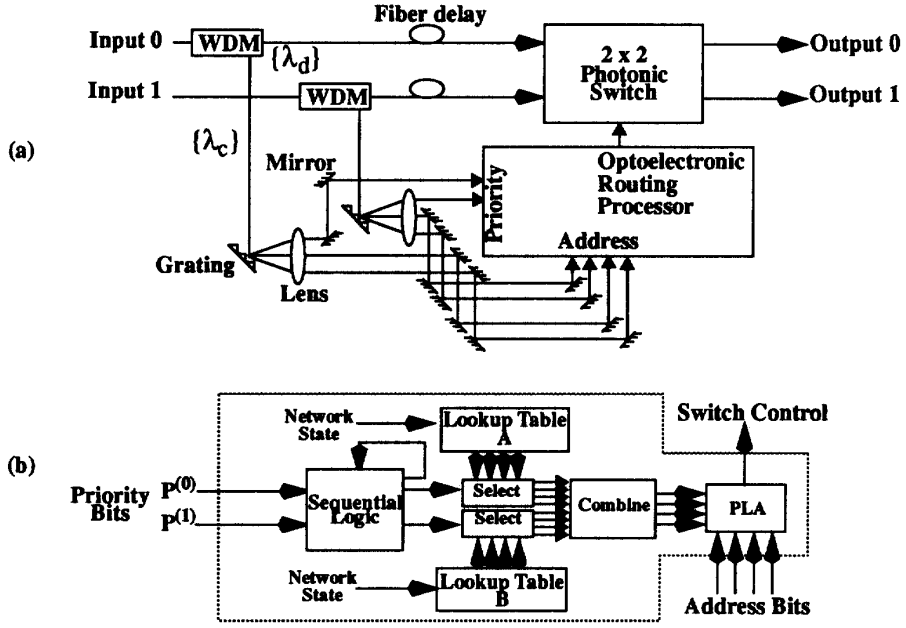
The electrooptic RCP is shown in Figure 1b. It processes the priority bits at a sequential stage in order to choose the routing function via lookup table A or B. The correct mapping is sent to a

GaAs programmable logic array (PLA) which is updatable at the packet rate and has a 2 ns access time. The PLA maps the four address bits to the correct control signal. Network state information can be used to change the lookup tables at a slower rate, providing reconfigurability on two different time scales.

## 2.0 Summary

We have demonstrated a novel reconfigurable photonic switch architecture which computes routing and contention resolution on the fly according to dynamically programmable lookup tables. Reconfigurability is at the word-size packet rate (> 10 Mpackets/sec) and latency is reduced to a single packet duration using GaAs technology. Details of the optoelectronic processor and resulting performance will be discussed.

**FIGURE 1. Architecture of a reconfigurable photonic switch with contention resolution**




## 3.0 References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