

A Multihop 2x2 All-Optical Photonic Packet Switch

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Abstract

In this paper we describe an all-optical packet switch architecture and present experimental results of all-optical multihop routing using 2x2 photonic packet switches. The switch is designed for distributed switching systems. At each hop, the full functions of self-routing, contention resolution, and header regeneration/reinsertion are performed with both switch inputs active. These results demonstrate a basic level of functionality needed to build full scale all-optical packet switched networks. Deflection routing is used to arbitrate contention. Three hops without optical amplification is demonstrated at a switch throughput of 36.4 Mpackets/sec, 145.6 Mbits/sec with a four bit payload. WDM out-of-band signaling is used to code and process the packet control header.

1 Introduction

Photonic packet switches have gained increasing attention in high bandwidth applications such as telecommunications and computer communications due to their bandwidth transparency. An "All-optical" multihop network, where the payload remains optical from source to destination, is an attractive approach since the payload can be routed independent of data rate and format. Presently, it is not practical to use optical memory as input buffers for all-optical switches. Bufferless architecture are a good preserve the optical bandwidth and reduce the need for switch buffers. Extremely simple routing protocols are required in order to allow the routing electronics to keep up with the optical payload.

An important building block is the 2x2 packet switch,

which can be used to build larger centralized switches or distributed switches with network access points. The architecture described in this paper is designed for a distributed switching environment. A fully functional switch must have the capability to route packets, resolve output-port contention, and in many cases compute a new header or update a portion of the current header. Modifying of the header is important with certain routing techniques such as deflection routing and ATM cell routing. Additionally, routing in multihop networks requires that packets traverse an unknown number of switch nodes. Therefore, header reinsertion must be independent of the lifetime of the packet in the network.

Previous work in this area include self-routing in 1x2 switches [1], and contention resolution in a 2x2 switch with both input-ports active [2]. A switch that used a single-packet active fiber-loop input buffer was able to handle limited cases of contention resolution [3]. Single pass header reinsertion in a 1x2 switch for ring networks has been reported in [4, 5] but did not have the capability to perform an arbitrary number of reinsertions.

The work presented in this paper represents the first time that the combined functions of real-time header regeneration/reinsertion, self-routing, and contention resolution have been demonstrated for multiple switch passes without performing opto-electronic conversion on the payload. Packets are routed through a 2x2 photonic packet switch with both input-ports active. The task of header reinsertion is greatly simplified by transmission the packet header on a separate waveband than the payload. The packets are coded bit-parallel using an novel one bit per wavelength code, eliminating the need for a start and stop signal [6].

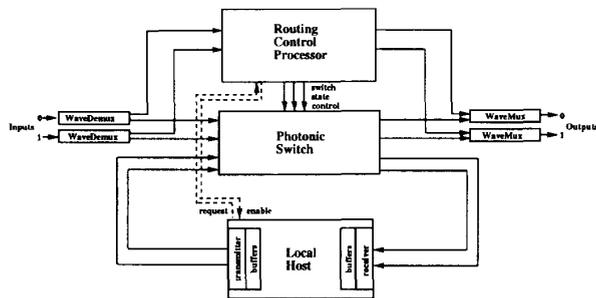


Figure 1: A photonic packet switching node for distributed multihop “all-optical” interconnects. Solid lines indicate fiber optic connections and dashed lines indicate electronic connections.

2 Switch Architecture

A conceptual model for a 2x2 photonic packet switch with local network access is shown in Fig. (1). This switch node is designed for a network of degree 2 and can be used to construct larger *indirect* switches for centralized switching or *direct* switches for distributed switching with local host access [7]. The node consists of a series of 2x2 switching fabrics and a routing control processor (RCP). As packets enter the switch, the out-of-band header is extracted using a wavelength demultiplexer. This technique is used in reverse to reinsert the header at the switch output, reducing the burden on timing requirements as compared to time division multiplexing techniques. Request and enable signals from the RCP allow the host to access the network through the photonic switch. The switch state control signals result from mediation of the network links with the local host. Contention for the host can be reduced through the use of parallel access ports at the switch output.

2.1 A 2x2 building block

In this paper, we discuss an experiment that demonstrates the functionality of a switch node without local network access. This reduced problem is shown schematically in Fig. (2). Packets enter the switch synchronously or asynchronously dependent on the overall network architecture. The payloads are separated from headers and temporarily delayed in static fiber delay lines in order to compensate for RCP latency. The RCP generates a switch state control signal and new packet header information. New header information is reassembled with the outgoing packets using static fiber delay lines for alignment.

2.2 Routing protocol

Deflection routing is used to arbitrate contention for switch output-ports [8]. Routing decisions are based on packet destination addresses and packet priorities. When packets entering

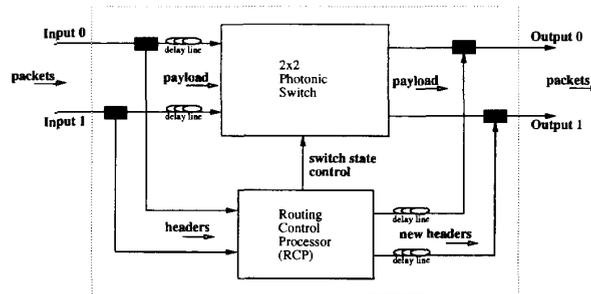


Figure 2: A 2x2 photonic switch building block.

the switch are destined for the same output port, those with higher priority are directed to the desired output-port and the remaining packets deflected to the other output-port. It is assumed that the network topology is multipath and recirculating such that packets can reach the destination via an alternate path (e.g. ShuffleNet, Manhattan Street). Deflected packets may have their priority increased in order to decrease the probability of deflection at the next switch. The outgoing header information is updated to reflect a change in priority.

Output-port contention with equal priorities requires fair arbitration and can lead to system livelock. In [2], the switch was maintained in its previous state under this condition. In [9], this condition is resolved by maintaining priority from packets entering the switch during the previous clock cycle. While the former technique yields a random allocation between input ports, the later technique will grant priority to one input for bursty periods of time, yet can change between the two inputs over time.

3 Experiment demonstration

In this section we describe multihop operation of a 2x2 photonic packet switch. The switch routes packets coded as six parallel wavelengths, two out-of-band control bits and four payload bits (see the optical spectrum analyzer output in Fig. (3)).

A diagram of the experimental switch is shown in Fig. (4). New optical header information is inserted in real-time with the outgoing payload at one of the switch output-ports (for demonstration purposes). The new header consists of a new address and updated priority bit. Packets are initially inserted at input-port 0 at a rate equal to the feedback delay between output-port 1 and input-port 1. The receiver at output-port 0 demultiplexes the individual payload bits in order to recover the payload. Output-port 1 is directly connected to input-port 1 through an optical fiber delay in order to demonstrate multihop routing by passing packets through the switch multiple times and simulate contention. Each payload contains packet identification information (i.e.

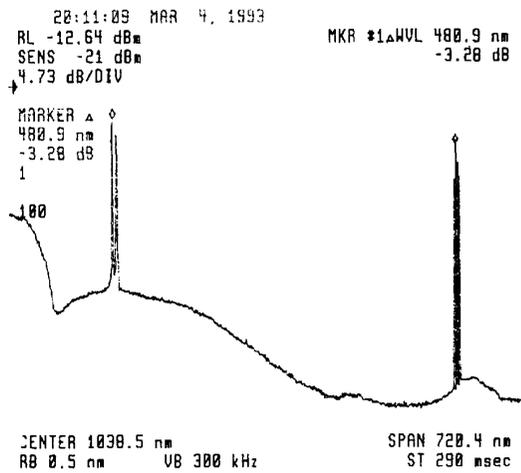


Figure 3: Out-of-band signaling in a bit-parallel packet. Two control bits at 830 nm and four payload bits at 1310 nm. The x-axis is increasing wavelength to the right.

packet one contains the number one, etc), and is generated using four DFB lasers temperature tuned to 1304.2, 1306.5, 1308.8, and 1310.1 nm. The original header is generated using two single mode lasers tuned to 826 and 828.4 nm and the reinserted header generated with two lasers tuned the same. The clock is distributed electronically from the transmitter to the switch, and in the future could be transmitted on a separate wavelength between switches.

3.1 Results

The deflection routing protocol was verified by viewing the bit parallel input headers, the resulting switch control state,

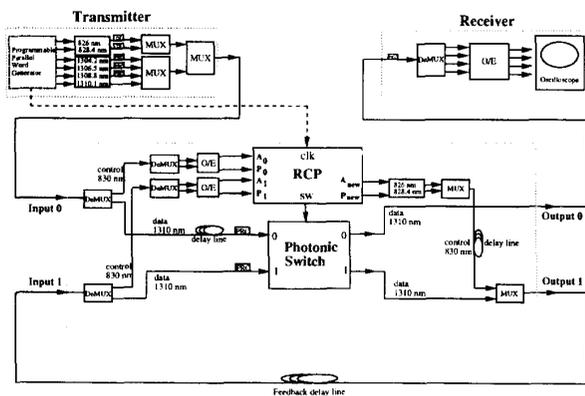


Figure 4: Experimental Setup of 2x2 photonic switch.

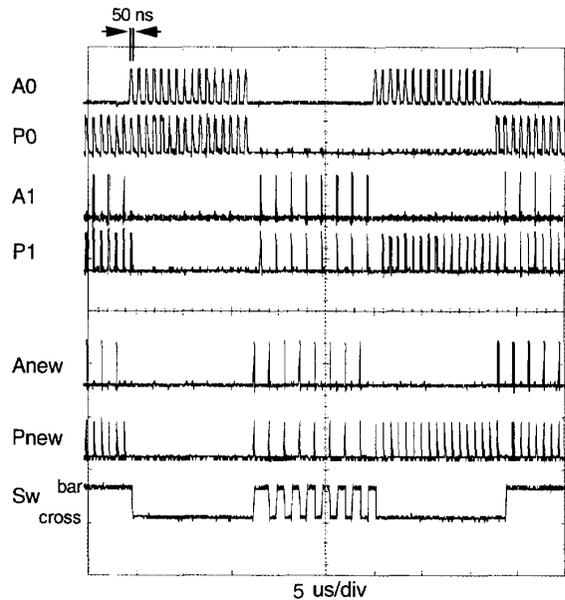


Figure 5: Verification of RCP operation

and the new address and priority bits for output port 1, and is shown in Fig. (5). A_0 and P_0 are the address and priority bits of input port 0 and A_1 and P_1 are the address and priority bits of input port 1. A_{new} and P_{new} are the new address and priority bits that are reinserted with the payload at output port 1 and appear as A_1 and P_1 at the next clock cycle. The combined losses from input port 0 to input port 1 through the feed back loop were measured at -13dB.

Two separate experiments were performed to verify overall system operation and test the maximum number of hops without optical amplification with the results shown in Fig. (6). Fig. (6)b illustrates three hop routing of payloads with two bits. The following packets were sent cyclically using the convention [data bit 0, data bit 1, address, priority]: [1,0,0,1][0,1,1,1][1,1,1,1], causing the packets to correctly appear at output-port 0 in the order 1,3,2, verifying three switch hops without optical amplification. In Fig. (6)a, only three bits of a four bit payload are shown due to problems with one of the photoreceivers. Seven packets were sent cyclically [1,0,0,0,1]; [0,1,0,0,1]; [1,1,0,1,1]; [0,0,1,1,1]; [1,0,1,1,1]; [0,1,1,0,1]; [1,1,1,1,1]. The packets arrive at output-port 0 in the order 1,2,7,3,5,4,6 as expected. Packets 1,2, and 5 traverse the switch once, packets 3 and 6 traverse the switch twice, and packets 4 and 7 are attenuated after three and four passes of the switch respectively and are not visible due to power budget losses measured at -13dB per switch pass. The throughput per input-port is 18.2 Mega-packets-per-second (MP/s) cor-

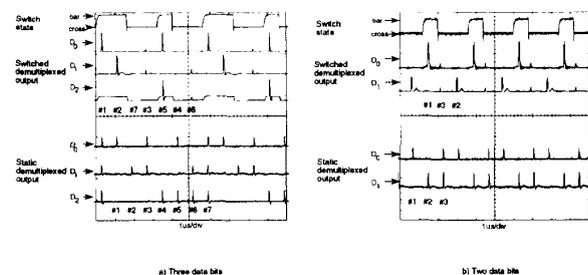


Figure 6: Demultiplexed switch outputs

responding to an aggregate switch throughput of 109 Mb/s for three bit packets and 145.6 Mb/s for four bit packets.

The routing decision time, including demultiplexing delay, detection delay and RCP delay was approximately 100 ns. Although packets were injected at a rate determined by the feedback path length, the maximum packet rate is currently determined by the bit duration of 50 ns. Assuming a guard band of 5 ns per packet to account for finite switching times and other uncertainties, the throughput per input-port is 18.2 Mega-packets-per-second (MP/s) corresponding to an aggregate switch throughput of 109 Mb/s for three bit packets and 145.6 Mb/s for four bit packets. The laser drivers and receivers we used are capable of 500 ps risetime operation. Implementation of the RCP in ECL would allow 5 ns bits plus 5 ns guardband yielding a potential switch throughput of 200 MP/s or 800 Mb/s for a three bit packet. Addition of more lasers will increase this throughput proportionally.

Limitations to the system include chromatic dispersion and bit skew (where the packet itself broadens due to mismatch in group velocity between bits), both of which can be compensated for using negative dispersion techniques. The individual laser channel power is also limited by nonlinear optical crosstalk due to channel power, number of channels, and distance traversed. Build up of ASE is also an important consideration and a topic for future research as more data bits are added and optical amplification utilized.

4 Summary

In this paper we have described multihop operation of a 2x2 photonic packet switch with header reinsertion and contention resolution. This switch is a building block for both centralized and distributed switch architectures. The switch routes multiple optical wavelengths simultaneously as demonstrated by the switching of bit parallel payloads. Simple TTL electronics were used to implement the routing control processor. The electronics run at the packet rate due to WDM transmission of bit-parallel packets. The throughput per input-port is 18.2 Mega-packets-per-second (MP/s) corresponding to a potential aggregate switch throughput of 109 Mb/s for three bit

packets and 145.6 Mb/s for four bit packets. This throughput can be increased by implementing the RCP in faster gate technologies and/or by adding more bits to each packet. Packets were shown to traverse the switch up to three times and circulate up to two times around the fiber feedback loop before excess losses limited detection. The excess losses per round trip switch pass were measured at -13dB. In a more mature system, optical amplifiers and optimized WDM components will be used to compensate for losses due to switching, coupling, and attenuation.

5 Acknowledgments

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