35 Gb/s Monolithic All-Optical Clock Recovery Pulse Source

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Abstract: We demonstrate clock recovery at 35 Gb/s from the first mode-locked laser integrated on-chip with input and output SOAs. Tuning one DBR mirror can change the output pulsewidth between 6.7 and 9.3 ps.

OCIS codes: (250.5300) Photonic integrated circuits, (140.4050) Mode-locked lasers

1. Introduction

Optical clock recovery (OCR) at high data rates is desirable for regeneration of data in fiber optic networks [1,2]. Mode-locked lasers (MLLs) have been investigated as a method of all-optical clock recovery with the advantage that they have a relatively compact and simple structure, and require no fast electronics under optical injection locking [1-3]. The output clock pulses can have higher power, better shape, and lower jitter than the input pulses [1]. The pulsewidth of the clock can also be short, which is essential for optical gating. These facts make MLLs ideal for 3R regeneration (re-timing, re-shaping, and re-amplification).

It is desirable to be able to recover the clock with the lowest possible input power and the highest output power. The integration of an MLL with semiconductor optical amplifiers (SOAs) can decrease the required input power and increase the output power of the device, in addition to performing retiming and reshaping of the input pulses. It is also desirable to be able to control the output pulsewidth in order to optimize the output for both optical gating, which desires a narrower pulsewidth, and transmission, which desires a wider pulsewidth to avoid dispersion.

In this paper we present a monolithic optical clock recovery pulse source consisting of an input SOA, an MLL with DBR mirrors, and an output SOA, as shown in Figure 1. To our knowledge, it is the first MLL integrated with SOAs and the first MLL with two DBR mirrors which precisely determine the mode-locking frequency via lithography instead of cleaving [1-4]. The mirrors also allow the output pulsewidth to be tuned between 6.7 and 9.3 ps by changing the current in one DBR mirror. We also demonstrate pulsed optical clock recovery from an uncompressed (sinusoidal shaped pulses) 35 Gb/s RZ PRBS input stream, which is in contrast to other schemes that require pulse compression [1-4]. The input SOA reduces the input power required for clock recovery by 10 dB compared to the case with no input SOA and the output SOA can increase the output power of the device beyond that of the MLL alone by 12 dB. The versatile integration platform used may allow for further integration of more components to create complex photonic integrated circuits incorporating MLLs.

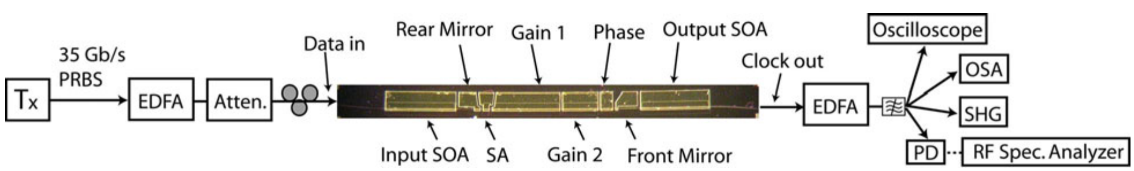

Fig. 1- Experimental setup with a photograph of the pulsed clock recovery device.

2. Device design

The device was fabricated on an InP substrate with InGaAsP offset quantum wells. This platform [5] allows for active regions and passive regions on the chip for reduced loss between components. The platform also allows for high-speed photodetectors and modulators, deeply etched regions for waveguide bends, and more [6]. The device was designed for 35 GHz operation due to system measurement limitations, but could easily be fabricated for 40 GHz or even much higher bit rates with a high precision in the locking frequency.

As shown in Figure 1, the device consists of a 550-µm long input SOA, an MLL, and a 550-µm long output SOA (referred to as "OutSOA"). The device's input and output waveguides are flared and curved for minimal reflections from the facets, which is critical for stable mode locking. The MLL consists of a 90% power reflecting rear input distributed Bragg reflector (DBR) mirror (R_{mirr}), a 50 µm saturable absorber (SA), a 550 µm gain section

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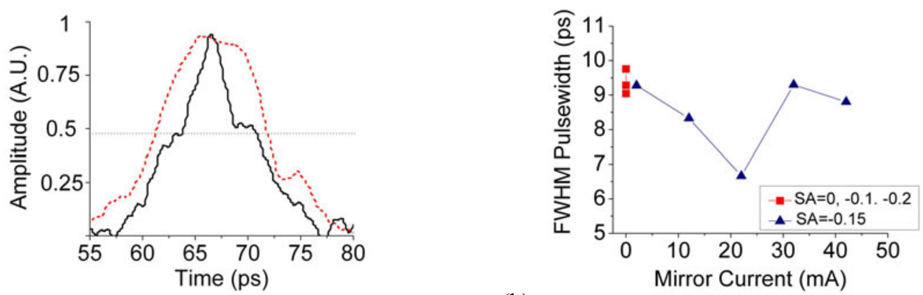
(G1), a 290 μm gain section (G2), a 100 μm long phase section (P), and a 40% reflecting front output DBR mirror. With 10-20 μm between contact regions for electrical isolation the MLL length is 1080 μm. The total device length is 3.5 mm. Based on experimental measurements in previously-made lasers, the group index is expected to be 3.95 so the expected resonant frequency of the MLL is 35.1 GHz. This is very close to the experimental value of 35.2 GHz shown in Figure 3(a). The rear mirror has a high reflectivity and is immediately next to the SA for optimal effect of the SA in self-colliding pulse mode locked operation [7]. The high reflectivity rear mirror reduces the input power to the MLL by about 10 dB and therefore the input power required for injection locking is higher than if injecting into the same side as the output. However this is necessary in order to effectively integrate the device because we must send data in one side and have the clock come out the other side. A colliding pulse MLL design would avoid highly reflective mirrors, but this instead requires that the cavity be twice as long [7].

3. Pulse shaping results

Figure 1 shows the experimental setup. First we tested the device's pulse shaping characteristics under passive mode-locking. In this case no input signal was sent into the device, and the laser output at 1550 nm was connected to a second harmonic generation autocorrelator (SHG), RF spectrum analyzer, and optical spectrum analyzer (OSA). Figure 2(a) shows SHG traces of the MLL pulses for two different bias conditions, resulting in over 3 ps difference in the full width at half maximum (FWHM) of the pulse. Some change in the pulsewidth occurs when changing the SA bias as shown in Figure 2(b). However, when the rear mirror is tuned relative to the front mirror the pulsewidth can be changed significantly. This is due to misalignment in the mirror spectra leading to fewer longitudinal modes lasing. This means the spectral width narrows and the pulsewidth broadens. We might expect the mirror spectra to be aligned with $R_{mirr}=F_{mirr}=0$, but uneven heating across the wafer causes different indexes of refraction in the two mirrors even without injection. By tuning the rear mirror current alone, we can tune that mirror into (R_{mirr}=22 mA) and out of (R_{mirr}=2 mA, 32 mA) alignment with the front mirror, changing the output pulsewidth between 6.7 and 9.3 ps as shown in Figure 2(b). Changing other laser bias conditions can further alter the pulsewidth.

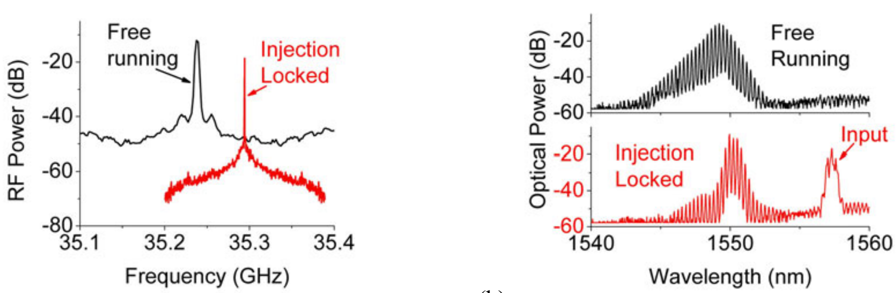


(a) (b)

Fig. 2- (a) Pulsewidths measured with an SHG for two different laser bias conditions: for the short pulse R_{Mirr}=22mA, SA=-0.13 V, G1=102 mA, G2=90 mA, P=23 mA, OutSOA=20 mA, for the wide pulse R_{Mirr}=0 mA, SA=-0.15 V, G1=132 mA, G2=90 mA, P=23 mA, OutSOA=60 mA. (b) Plot of FWHM pulsewidth versus the rear mirror current for SA=-0.13 V, G1=102 mA, G2=90 mA, P=23 mA, OutSOA=20 mA. Also shown are the pulsewidth variations with SA bias for the same bias conditions except R_{Mirr}=0. Increasing the SA reverse bias slightly decreases pulsewidth.

4. All-optical clock recovery results

When the data signal is injected into the device the jitter is reduced considerably [4] as indicated in Figure 3(a) by the RF spectrum narrowing. After injection the peak also shifts in frequency to align itself to the incoming data rate. Figure 3(b) shows the corresponding optical spectra along with the input data in the case of injection.



(a) (b)

Fig. 3- (a) RF spectra of the free running and injection locked (clock recovery) output from the device and (b) corresponding optical spectra.

The input data stream is shown in Figure 4(a). It is uncompressed and slightly distorted due to imperfect multiplexing. For these measurements, the input wavelength was between 1556 and 1558 nm. With data injected, the clock is recovered with the waveforms shown in Figure 4(b) and (c) for two different device bias conditions. In both cases, the recovered clock jitter is equal to that of the incoming data: 1.6 ps in (b) and 3 ps in (c). However, the laser's bias conditions significantly change the recovered clock pulsewidth, as seen in the waveforms. The corresponding optical spectra of the two recovered clock signals are also shown in Figure 4(d) and (e).

Next the required input power of the injected data was tested as a function of the input SOA current, while other bias conditions were fixed. The results are shown in Figure 4(f) left axis. This demonstrates a range of 10 dB when biased between minimum and maximum input SOA bias, implying that the SOA gives about 10 dB increase in input power compared to the laser without an SOA. If the bias conditions are changed, the clock can be recovered for input powers as low as -1 dBm. Finally, we tested the output power of the device as a function of the SOA current, with no data injection. These results are shown in Figure 4(f) right axis. The output power can be tuned from –7.8 dBm at transparency (20 mA on the SOA) to 4.6 dBm with 70 mA applied to the SOA. Beyond 70 mA, the laser becomes unstable and will not mode-lock unless other conditions are changed. With the output power of the device at 4.6 dBm and the required input at 4.5 dBm or less, some fiber to fiber gain is possible. Taking into consideration a total coupling loss of around 5 dB per facet, this device can recover the clock with over 10 dB gain on chip. With design improvements, we expect that more fiber to fiber gain is possible using this type of device.

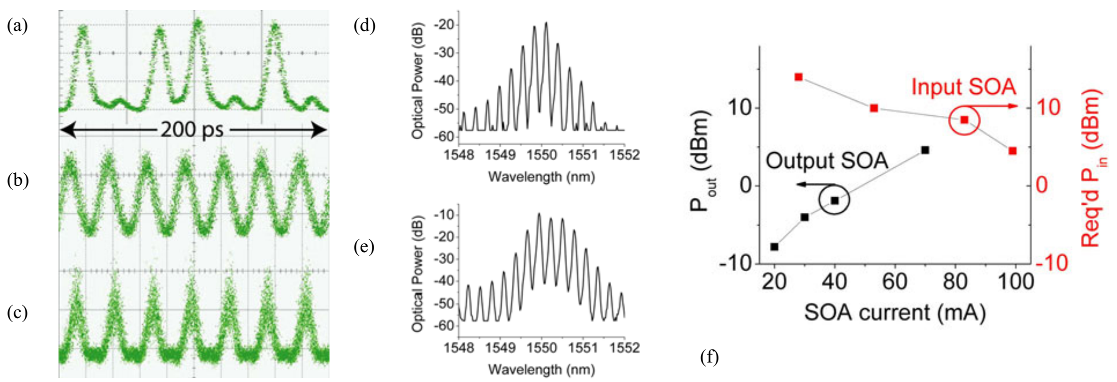


Fig. 4- (a) The uncompressed 2^{31}-1 PRBS input data stream with some distortion due to poor multiplexing, 1.7 ps RMS jitter. (b) and (c) Oscilloscope traces of the recovered clock for two different laser bias conditions. (d) and (e) OSA traces corresponding to (b) and (c) respectively. (f) Fiber coupled output power versus the output SOA current (left) for the same bias conditions as in Figure 2(b) except for the case with 70 mA, in which G2=68 mA and SA=-0.05 V. Also shown (right) is the required fiber coupled input power for successful clock recovery versus input SOA current for SA=open, G1=133 mA, G2=102 mA, P=11.25, OutSOA=110 mA.

5. Conclusion

We have demonstrated a monolithic pulse source consisting of a passively mode-locked laser combined with SOAs at the input and output of the device. By changing the bias conditions on the laser, the output pulsewidth can be tuned between 6.7 and 10 ps. Also by increasing the current on the input and output SOAs, the required input power and the output power of the device can both be improved by 10 dB compared to the case of a laser without SOAs integrated. The device was used to perform all-optical clock recovery on 35 Gbps RZ data with a 2^{31}-1 PRBS pattern by optically injection locking the device to the input data stream. The output clock is reshaped and has a tunable, relatively narrow pulsewidth ideal for gating. By further integration of this type of device, novel photonic integrated circuits may be possible. This work was supported by DARPA/MTO and ARL under the DoD-N program and LASOR project grant number #W911NF-04-9-0001 and 3R project grant #W911NF-06-1-0019.

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