Demonstration of contention resolution between two 40 Gb/s packet streams using multiple photonic chip optical buffers

Emily F. Burmeister, John P. Mack, Henrik N. Poulsen, Biljana Stamenić, Milan Mašanović, Daniel J. Blumenthal, John E. Bowers

ECE Department, University of California, Santa Barbara, California, USA 93106-9560

e-mail: {emily, jmack, henrik, biljana, mashan, danb, bowers}@ece.ucsb.edu

Abstract

Integrated optical RAM using InP switches with silica waveguide delays perform contention resolution with 99% packet recovery for 40-byte packets. Two buffered inputs and two packet depths are demonstrated.

Introduction

Optical router technology has the potential to address the power and footprint limitations of increasingly higher capacity electronic routers. However, a practical integrated optical buffer that can operate with the required signal fidelity and control interface is necessary to handle contention. To date, optical buffering has been reported using discrete technologies, which greatly limits the buffer performance, cost, and eventual depth. In this paper we report the first buffering demonstration of IP-sized packets by chip-scale optical memory for multiple input ports under scheduling control. The buffers ran autonomously using a payload envelope detect circuit to discern upcoming contention, an arbiter to make buffering decisions, and electronic channel processors to send signals to the buffer device. The optical RAM (random access memory) approach presented here is advantageous because it can store 40 Gb/s, 40-byte packets in a small footprint [1]. Delay line buffers have been reported with excellent performance [2], but chip-level integration and system demonstrations are necessary for optical buffering to become a reality.

Buffer design

Recirculating buffers have the advantage of requiring only one major component while providing dynamic control of storage times with the granularity of the delay line length. The buffers used in this work combine 2x2 InP-based switches with on-chip silica-on-silicon delay lines that are 2.65 m in length i.e. 12.8 ns delay (Fig. 1). The delay line length is chosen to be slightly longer than the length of a 40 Gb/s, 40-byte packet and its guard bands; thus allowing the greatest resolution in possible delay times.

The InP 2x2 switch meets the performance requirements to realize a recirculating packet buffer compatible at the system level. Our buffer design operates at 40 Gb/s, has high extinction ratios (>40 dB) for cascadability [3] and can switch in under 2 ns, which is within packet guard bands. The semiconductor optical amplifier (SOA) gate matrix switch is the best switch choice for recirculating buffers primarily because it provides high extinction while meeting the speed needs and compensates for splitter and delay line loss. Switching between ports is controlled by turning on and off the switching amplifiers placed at the center of the chip (Fig. 1a). The input light is split between the delay loop input and the output port and is amplified for the desired direction while the other half of the signal is absorbed by the quantum wells in the amplifier that is turned off. The fabricated switches met all of the performance requirements.

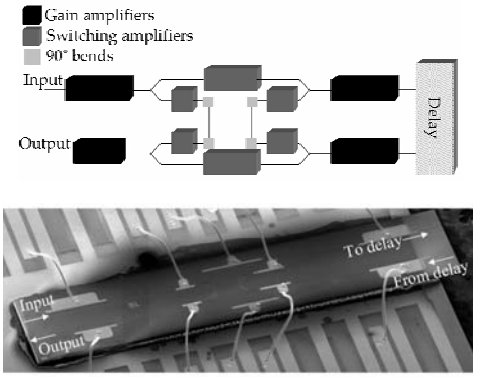

Figure 1: (a) Schematic of buffer device and (b) SEM of InP 2x2 SOA gate matrix switch.

Silica-on-silicon waveguides are used to provide a nearly transparent delay loop while being relatively compact. Passive measurements were taken over a wavelength range from 1525 nm to 1575 nm for the silica waveguides. Measurements show propagation losses of less than 0.04 dB/cm at 1550 nm, and varied less than 0.001 dB/cm over the 50 nm span. Polarization dependent loss for 200 cm of waveguide was approximately 1 dB and chromatic dispersion was approximately 130 ps/nm•km. The waveguide design is conservatively limited to a minimum bend radius of 6 mm, but was spiraled on the chip to reduce space. The area needed for 2 m of delay is 6.4 cm^2.

System demonstrations and results

The optical buffer was capable of holding a 40 byte, 40 Gb/s packet for up to 5 circulations, or 64 ns of delay, with greater than 98% packet recovery [4]. All packet measurements were performed using 2x2 InP switches on carriers, butt-coupled to the silica waveguide devices. To generate 40 Gb/s packets, a CW (continuous wave) optical signal (1560 nm) was modulated using an SHF 50 Gb/s BERT (bit error rate tester) with RZ (return-to-zero) data in 40-byte packets that contain identifier bits for packet recovery measurements. Packets were considered recovered if the entire 64-bit string was error-free.

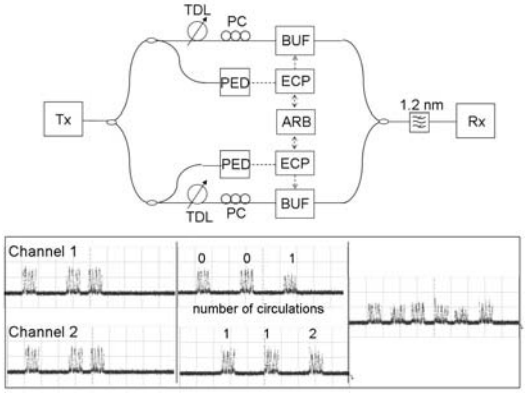

Figure 2: (a) Testing diagram for 2 buffered streams and (b) oscilloscope traces showing packets.

Buffered 2-channel contention resolution under autonomous control was demonstrated. To enable autonomous operation, half of the incoming data was split to payload envelope detect (PED) circuits that give the 2 electronic channel processors (ECP) knowledge of packet arrival (Fig. 2a). Each ECP sends port requests to the arbiter board (ARB) which tracks the packets and makes buffering decisions. The ECPs send gating control signals to the optical buffers for read, write, or bypass state operation. A stream of three packets was used to exercise several buffering states (Fig. 2b). The sensitivity packet measurements show that all packets had greater than 99.5% packet recovery.

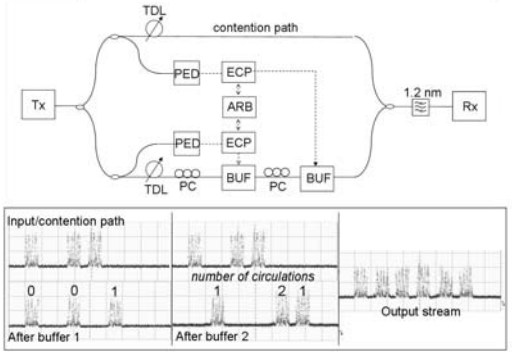

Figure 3: (a) Testing diagram for two in-line buffers and (b) oscilloscope traces showing packets.

The second experiment demonstrated the use of 2 on-chip optical buffers in-line on 1 packet stream to provide contention resolution for a second stream. The firmware in the arbiter was changed to reflect the new positions and roles of the buffers (Fig. 3a). The same stream of three packets was sent through the first buffer where the third packet was buffered for one time slot. The stream then passed through the second buffer which delayed the first and third packet for one time slot and the second packet for two time slots (Fig. 3b). Greater than 99% packet recovery was measured for all packets (Fig. 4).

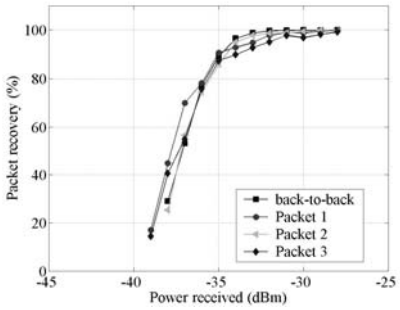

Figure 4: Packet recovery for in-line demonstration.

Conclusions

This work presents the first use of integrated optical random access memory (ORAM) packet buffers to provide contention resolution for a 40 Gb/s packet stream. The optical buffers had greater than 98% packet recovery for up to 5 circulations, or 64 ns of delay. System level demonstrations were conducted for two configurations: two buffered inputs with single packet deep buffers and one buffered input with a two packet deep buffer. The autonomous contention resolution was performed with 40 Gb/s, 40-byte packets with greater than 99% packet recovery, demonstrating a realistic buffering technology to overcome a major challenge in optical router development. The optical buffers reported in this work provide an integrated solution to meet the predicted memory needs in core optical routers [5].

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