Photonic Integrated Circuit Switch Matrix and Waveguide Delay Lines for Optical Packet Synchronization

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Abstract

The first integrated synchronizer is demonstrated using silica delays coupled to an InP switch. Error-free performance is presented for delays of 0, 2.96, 6.56 and 9.52ns.

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Introduction

Optical packet switching (OPS) is a potential solution to achieving high capacity routing while addressing the impending power and footprint limitations of ultra-high capacity electronic packet routing systems [1]. Packet based networks scale well due to their asynchronous nature [2]. A major challenge in implementing OPS is to handle asynchronous arrival of packets at multiple input ports at each node to support functions such as optical buffering and forwarding [3-4].

Synchronization has been previously reported with good performance using fiber delay lines [5-6], but an integrated solution has yet to be demonstrated. Choosing a synchronizer design that can be integrated is important for the scalability of optical packet switched routers because of reduced footprint, latency, and timing uncertainties. Chip-scale optical packet buffering has been demonstrated at 40Gbps with an InP switch and silica-on-silicon recirculating feedback delay line using similar technology [7-8]. In this work, we demonstrate for the first time a 2-stage feed-forward photonic chip for optical packet synchronization at 40Gbps.

Synchronizer Design

The demonstrated 2-stage synchronizer consists of an InP switch matrix coupled to silica-on-silicon delay lines as shown in Fig. 1. The synchronizer is intended to be used at the inputs of an optical router to align packets to time slots for switching. The InP switch operates at 40Gbps, has high extinction ratios (>40dB) and sub-nanosecond switching. The InP switch is butt-coupled to a silica-on-silicon chip to provide the delays necessary for synchronization. All of the chip inputs, outputs, and transitions from one substrate to the other are angled for low reflection loss. The various delays of the synchronizer are chosen by gating semiconductor optical amplifiers (SOAs). The amplifiers in the desired signal path are forward biased to provide gain while the remaining amplifiers are left off and absorbing. Ideally, the delays are multiples of the required resolution, Δ, and the resulting dynamic range is $(2^N-1) \times \Delta$ where N is the number of stages. The relative delays of the demonstrated synchronizer are 0, 2.96, 6.56, and 9.52ns and can be used to align packets to a local clock operating at approximately 100MHz.

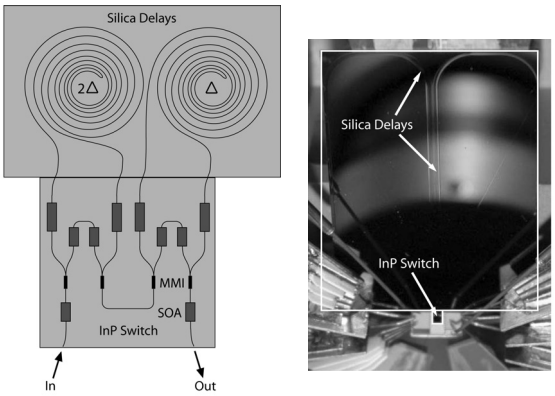

Figure 1: Photonic chip optical synchronizer

Measurements

The InP switch was soldered and wire bonded to an aluminium nitride submount and affixed to a copper mount using a thermal compound. The submount was maintained at a temperature of approximately 20°C. Lensed fibers were used to couple light in and out of the InP switch. The silica-on-silicon delay line chip was butt-coupled to the InP switch using a translation stage with six degrees of freedom.

A CW laser source operating at 1560nm followed by a variable attenuator and a polarization controller were used at the input of the synchronizer to conduct insertion loss (IL) and optical signal to noise ratio (OSNR) measurements. A bandpass filter with a bandwidth of 5nm was placed at the output of the synchronizer for the IL measurement. At an input power of -2dBm the insertion losses were 1.8, 4.2, 6.8, and 10.8 dB for the smallest to largest delays. The drive signals to the switches can be adjusted to account for the losses and provide a constant power output. An optical spectrum analyzer was used at the output of the synchronizer to measure OSNR by taking the difference of the peak power and the average of the noise +/- 1nm from the peak. The

initial OSNR for the source was 57.5dB. We observed that the OSNR decreased linearly for all delays for a range of input powers from -3 to 23dBm as shown in Fig. 2. The offset in curves for the various delays is due to the difference in insertion losses as well as the longer SOAs required for the delay paths which increases noise.

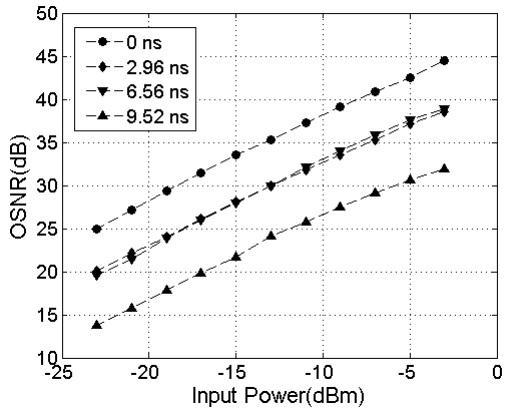

Figure 2: OSNR versus input power.

Bit error rate (BER) measurements were conducted for a range of input powers into the synchronizer using RZ 2^{31}-1 PRBS data at 40Gbps with the experimental setup shown in Fig. 3. The sensitivity degradation at 0dBm input power is shown in Fig. 4. The power penalty is greater than 2dB at 0dBm input power for longest delay due to the high insertion loss and degraded OSNR. The power penalty is less than 1dB for delays equalling 0, 2.96, and 6.56ns although there were patterning effects due to saturation.

Input power dynamic range measurements were conducted by varying the input power into the synchronizer and the results are shown in Fig. 5. For input powers less than -6dBm, the signal is degraded due to noise. As the input power is increased the power penalties for delays equal to 0, 2.96, and 6.56ns reach a minimum around -4dBm. We conclude that neither saturation nor noise is a significant issue for this set of operating conditions. As the input power increases saturation of the SOAs takes place which leads to increased power penalties due to patterning effects. The input power dynamic range is greater than 15dB for delays equal to 0, 2.96, and 6.56ns.

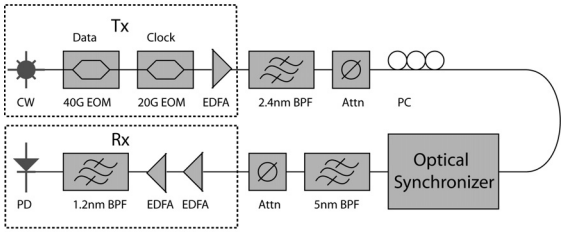

Figure 3: Experimental setup for BER measurements

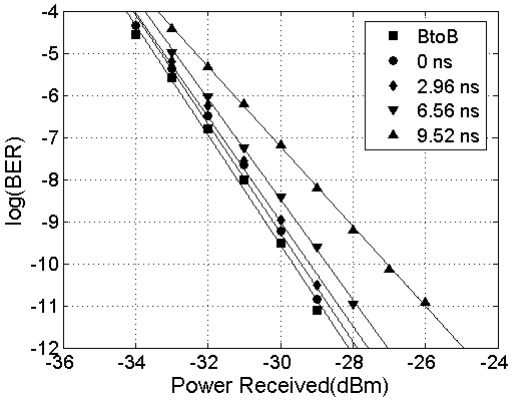

Figure 4: BER vs. received power at 0dBm input power.

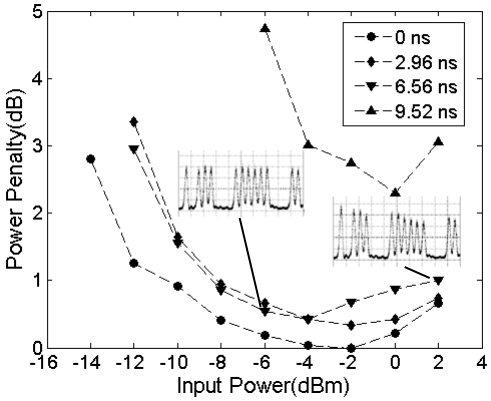

Figure 5: Input power dynamic range measurements.

Conclusions

We report the first demonstration of a 2-stage photonic integrated circuit for optical packet synchronization at 40Gbps. Error-free performance was achieved for all possible delays equalling 0, 2.96, 6.56, and 9.52ns. In the future, the SOA lengths can be increased in order to provide more gain for the chip. Mode converters can be applied to the InP switch to reduce coupling losses due to the mode mismatch between the two chips. Also, changing the current to the SOAs for the different delays can eliminate the variation of insertion losses.

Acknowledgements

This work was supported by DARPA/MTO and ARL under LASOR award #W911NF-04-9-0001.

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