Synchronously Loaded Optical Packet Buffer

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***Abstract*—Synchronous optical packet buffering is demonstrated utilizing a fiber-based synchronizer with a photonic integrated circuit packet buffer. Asynchronously arriving packets are optically synchronized to a local frame clock and loaded synchronously into the optical buffer. The synchronizer is a four-stage design with a resolution of 853 ps and a dynamic tuning range of 12.8 ns. The optical packet buffer consists of an integrated 2 × 2 InP switch coupled to a silica-on-silicon 12.8-ns delay line. Packet recovery measurements of 40-B return-to-zero packets at 40 Gb/s show-error free performance for several combinations of synchronizer and buffer delays.**

***Index Terms*—Buffers, optical memories, optical switches, packet switching, synchronization.**

I. Introduction

OPTICAL packet switching (OPS) provides a means of communication that is flexible, scalable, fast switching, and high capacity [1]. Two major challenges of OPS are dealing with the asynchronous nature of packet arrival and contention resolution [2], [3]. In real scalable optical networks, switches must operate asynchronously with respect to other nodes and packet sources [4]. This requirement results in packets arriving misaligned with the local clock as well as with other packets on the same input and different inputs of switch nodes. In order to efficiently utilize node output links and support packet buffering, it is necessary to align incoming packets to the local clock.

Optical packet synchronizers and buffers have been demonstrated utilizing wavelength conversion and semiconductor optical amplifier (SOA)-based switches [5]–[9]. While the former minimizes the number of active components required the latter is more compact and amenable to integration. Synchronization of 40-B packets at 40 Gb/s has been demonstrated previously using a fiber-based synchronizer [10]. Contention resolution has been demonstrated using a fiber-based buffer with asynchronous operation at 40 Gb/s [11]. Buffering with an integrated switch and fiber delay has also been demonstrated at 40 Gb/s [12]. The buffer used in this work consists of photonic chips that operate at 40 Gb/s [13]. Integration of the demonstrated synchronizer can be achieved through the same technology used for the buffer [14].

In this letter, we report for the first time a synchronously loaded optical packet buffer operating at 40 Gb/s. Asynchronously arriving packets are optically synchronized on a per packet basis to a local frame clock. Packets are then synchronously loaded into an integrated optical packet buffer which can be used for contention resolution.

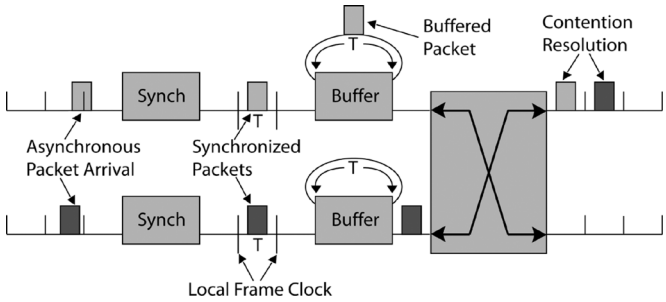

Fig. 1. Packets arrive asynchronously to optical switches. Synchronous buffers align packets to a local frame clock and resolve contention.

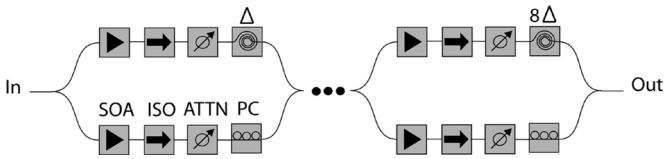

Fig. 2. Fiber-based four-stage synchronizer with SOA gates. (ISO: isolator. ATTN: attenuator. PC: polarization controller.)

II. Synchronizer and Buffer Design

The challenge of asynchronous packet arrival and contention resolution is illustrated in Fig. 1. Packets arrive asynchronously at the inputs of optical switches and are aligned to the local frame clock of the switch through the use of optical synchronizers. Packets are then synchronously loaded and unloaded from optical buffers to resolve temporal collisions of packets contending for the same output port.

The demonstrated synchronizer is based on a feed-forward design that utilizes bulk SOAs and fiber delay lines as shown in Fig. 2. A combination of SOAs was used as the gates to select the delay and compensate for losses. Polarization controllers were placed in each stage so that all delays had the same polarization rotation to match the transverse-electric polarization dependence of the buffer. The attenuators were tuned so that the insertion losses for the various paths were as close as possible with less than 2 dB maximum difference. The delay tuning range was chosen to match the size of the buffer or period of the local frame clock running at 78.125 MHz equivalent to a period of 12.8 ns. A four-stage synchronizer was chosen to provide a small enough resolution to compensate for the rise and fall times of the SOAs in the buffer. The relative delay through any configuration of the synchronizer can be given as $T(n) = n \times \Delta$ $(n = 0, 1, 2 \ldots 15)$, where $\Delta = 853$ ps and the delay tuning range is 12.8 ns.

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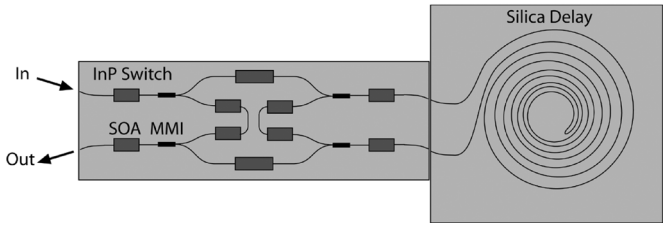

Fig. 3. Integrated buffer with InP switch butt-coupled to 12.8-ns silica-on-silicon delay line. (MMI: 1 × 2 multimode interference splitter.)

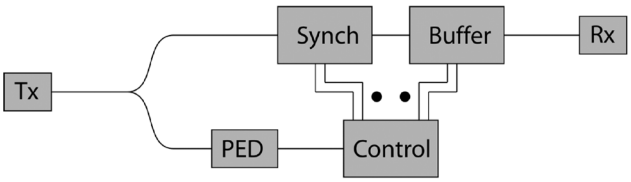

Fig. 4. Experimental setup of synchronously loaded packet buffer.

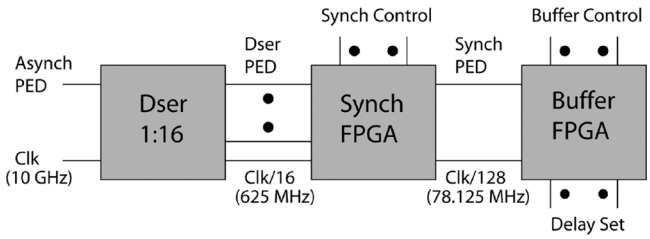

Fig. 5. Electronic control consists of PED, 1 : 16 Dser, synchronizer FPGA, and buffer FPGA.

The buffer used in this experiment is a feedback design that combines an integrated 2 × 2 InP offset quantum-well SOA-based switch butt-coupled to a silica-on-silicon delay line equivalent to 12.8 ns, as illustrated in Fig. 3. The switch operates at 40 Gb/s, has high extinction (>40 dB), low cross-talk (< −40 dB), and fast switching times (<2 ns). The delay line was chosen to be slightly longer than a 40-B packet (8 ns) at 40 Gb/s and 2-ns guard bands determined from the switching times of the SOAs.

III. Performance Measurements

The experimental setup designed to test the dynamic tuning capabilities of the synchronizer and buffer is depicted in Fig. 4. In this experiment, 40-B return-to-zero packets at 40 Gb/s are used as the data. Each packet consists of a 32-bit idler, 64-bit identifier, 8-bit label, and repeated pseudorandom binary sequence $2^7 - 1$. The data stream was engineered to test all states of the synchronizer. The data stream consists of 16 packets where each packet is spaced by $T\ (n) = 102.4\ \text{ns} + n \times \Delta$ $(n = 0, 1, 2 \ldots 15)$ and the total period equals 2.048 μs. The skew relative to the local clock of the incoming asynchronous packets corresponding to $T(5)$ and $T(10)$ are shown in Fig. 6.

The electronic control consists of a payload envelope detector (PED), a deserializer (Dser), a synchronizer field-programmable gate array (FPGA), and a buffer FPGA as shown in Fig. 5. The transmitted signal is tapped for electronic control processing. The PED is used to detect incoming asynchronous packets and generate packet envelopes as can be seen in Fig. 6. The PED consists of a 10-GHz photodetector followed by a 2.5-GHz limiting amplifier. The envelopes enter a 1 : 16

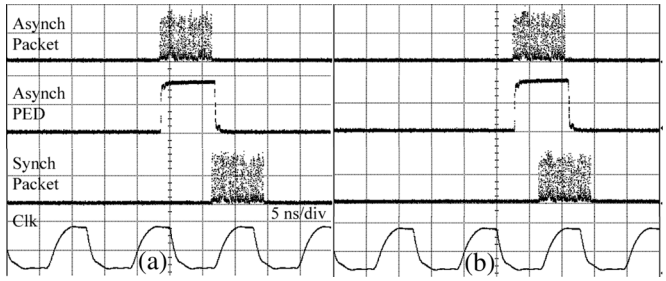

Fig. 6. Screenshots of asynchronous packet arrival, recovered asynchronous PED, synchronized packet, and local clock (a) Synchronizer delay of $T(10)$. (b) Synchronizer delay of $T(5)$.

Dser board operating at 10 GHz which allows the rising edge of the packet to be sampled within 100 ps. The deserialized envelope enters the synchronizer FPGA-based board where it is further deserialized from 16 : 128 channels so that it can be processed in parallel by the 78.125-MHz local clock. In this experiment, the 10-GHz and 78.125-MHz clocks were derived from the transmitter to avoid the use of high-speed clock recovery circuits which would be necessary if the control plane and transmitter were operated asynchronously. Here 16 channels of the deserialized data are used which correspond to the delays of the synchronizer. The deserialized data is compared to the rising edge of the local frame clock to determine the delay needed to align the packet to the clock. The FPGA generates SOA control signals which correspond to the delay determined to synchronize the packet. If no envelope is detected then the FPGA turns off all SOA control signals. The control signals are expanded to 38.4 ns through set–reset (SR) latches in order to gate the packets. The signals are then latched through D flip flops in order to match the total delay of each stage of the synchronizer. Thereby, the packets are delayed accordingly and synchronized to the local frame clock within 853 ps. Packets with delays equal to $T(10)$ and $T(5)$ are shown in Fig. 6.

The detected payload envelopes are fed through a D flip flop so that they are synchronous to the local clock and then are forwarded to the buffer FPGA along with the local clock. The buffer FPGA uses the synchronous payload envelopes along with the user defined delay to set the number of circulations the packets will experience and generate control signals for the buffer. A fixed fiber delay of 2.4 ns relative to the clock was placed after the synchronizer to meet the guard band requirements of the buffer. Synchronous packets with synchronizer delays equal to $T(10)$ and $T(5)$ and buffer delays of zero, two, and four circulations are depicted in Fig. 7.

Layer-2 (packet recovery) measurements were conducted for synchronizer delays of $T(10)$ and $T(5)$ and buffer delays corresponding to zero, two, and four circulations. The results are shown in Fig. 8. Error-free performance was achieved for both synchronizer delays and buffer delays of zero and two circulations with a power penalty less than 1 dB. Measured negative power penalties were obtained for some states due to the gating of SOAs, the misbalance of insertion losses in the synchronizer, and the use of a preamplified receiver. Performance improves from zero to two circulations due to increased optical signal-to-noise ratio (OSNR) as previously demonstrated for the buffer. Although error-free performance for four circulations was not possible, greater than 97% packet throughput was shown. The reason for an error floor is due to accumulated

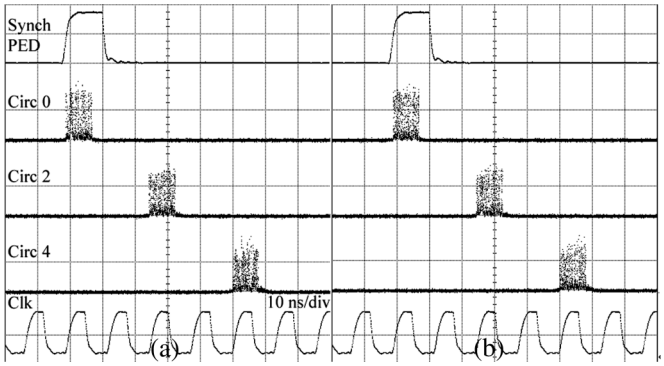

Fig. 7. Screenshots of synchronous PED, buffer circulations of zero, two, and four, and local clock. (a) Synchronizer delay of $T(10)$. (b) Synchronizer delay of $T(5)$.

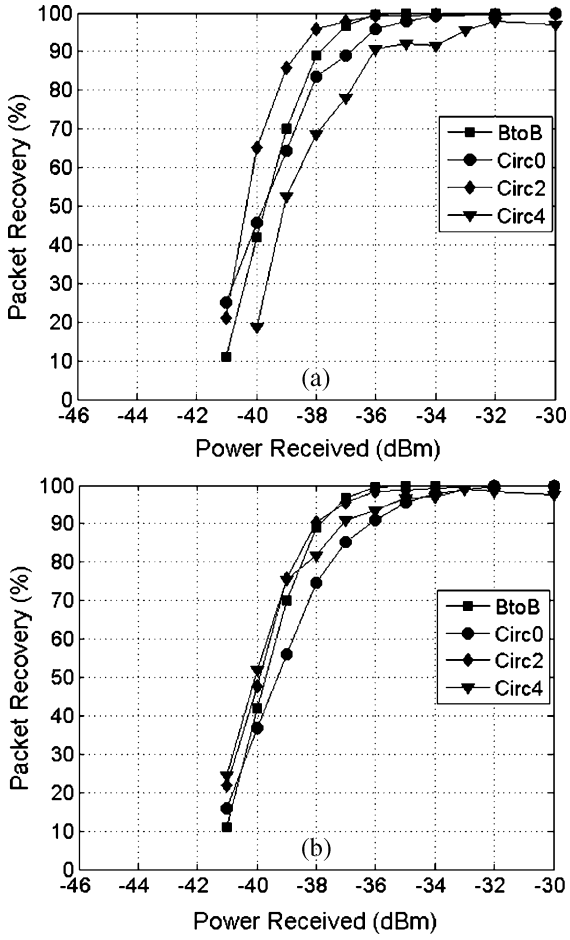

Fig. 8. Packet recovery measurements of synchronous buffer. (a) Synchronizer delay of $T(10)$. (b) Synchronizer delay of $T(5)$.

amplified spontaneous emission caused from cascaded SOAs in the synchronizer and buffer which reduces OSNR. An increased number of circulations can be achieved through the use of a bandpass filter or regeneration in the buffer.

IV. Conclusion

This letter reported on the first synchronously loaded optical packet buffer operating at 40 Gb/s. The synchronous buffer consisted of a fiber-based synchronizer followed by an integrated packet buffer. Autonomous synchronous buffering was demonstrated using a PED, Dser, and FPGA-based boards for electronic control. The synchronizer aligned asynchronously arriving packets to a local frame clock so that they could be loaded and unloaded from the buffer synchronously. Without synchronization, the incoming asynchronous packets could be either lost by SOA gating or misaligned when loaded and unloaded from the buffer. Packet recovery measurements for several combinations of synchronizer and buffer delays were conducted and greater than 97% throughput was realized.

Future improvements can be made to the synchronously loaded buffer to increase performance. The demonstrated synchronizer can be integrated utilizing the same technology used in the buffer. Polarization dependence can be reduced by using bulk SOAs in the buffer. The number of circulations achievable can be increased by placing a thin-film filter in the delay line of the buffer. Finally, the integrated delay line in the buffer can be replaced with a fiber delay for use with variable length packets.

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