Synchronous Optical Packet Buffers

John P. Mack, Emily F. Burmeister, John M. Garcia, Henrik N. Poulsen, Biljana Stamenic, Geza Kurczveil, Kimchau N. Nguyen, Kurtis Hollar, John E. Bowers, *Fellow, IEEE*, and Daniel J. Blumenthal, *Fellow, IEEE*

***Abstract*—Synchronous optical packet buffering is presented as a solution for asynchronous time division multiplexed (TDM) optical packet switched networks. Truly asynchronous optical packet synchronization and buffering are demonstrated using multiple independent transmitters, synchronous optical buffers, and a burst mode receiver. Optical packet synchronizers are used to dynamically align incoming asynchronous packets to local timeslots for synchronous loading of buffers. Multiple optical buffers based on integrated InP technology resolve contention of packets destined for the same output port at the same time. TDM asynchronous optical packets are detected on a per packet basis using a burst mode receiver with better than 99.9% packet recovery. An analysis of power consumption of the synchronous buffers is presented and potential power reductions are discussed.**

***Index Terms*—Buffers, optical communication, packet switching, semiconductor optical amplifiers, synchronization.**

I. Introduction

OPTICAL packet switching (OPS) provides a means of communication that is flexible, scalable, fast switching, high capacity, small footprint, and low power consumption [1]. In label switched optical packet switching, one approach to forwarding is to transmit lower bit-rate optical labels attached to high bit-rate optical payloads [2]. This allows for the use of low frequency electronics for processing label information while transparently forwarding high bit-rate payloads optically at low switching speeds [3]. Furthermore, burst mode optics can be used where energy is expended only when high speed data is present, and has the potential to reduce overall power consumption. The use of low-speed electronics and further integration of burst mode photonic devices could reduce power and footprint limitations of scaling high capacity data routers.

Asynchronous operation of routers is the key for the scalability of large scale systems or networks. However, there has been very little work published on asynchronous operation in the field of optical packet switching where multiple independent nodes are used, each with their own packet and bit-level clock. Asynchronous operation creates inherent timing uncertainties on the clock and packet-level due to the frequency drift between plesiochronous clocks [4], [5]. This causes packets to arrive asynchronously at the inputs of routers. Consequently, synchronization techniques are needed to align asynchronous packets in time for efficient buffering and switching [5], [6]. The use of synchronizers improves throughput and channel utilization as synchronization guarantees minimal skew between packets on different input ports. Routers require buffers to resolve contention of packets simultaneously destined for the same port [7]–[9] In electronic routers, synchronization and buffering of packets is done through the use of random access memory (RAM) where individual bits can be stored indefinitely and read at any time. However, the equivalent of electronic memory has not yet been realized in the optical domain, so achieving optical synchronization and buffering is a challenging task.

A unique aspect of optical packet switching is that payloads are switched on the packet-level, not the bit-level. This means that optical techniques can be employed where entire packets are delayed in time [5], [7]. The most straightforward and realized approach to optical synchronization and buffering is through using fiber or waveguide delay lines where photonic switches are used to select the delay needed to align packets in time and resolve contention [10]–[19]. Optical synchronization and buffering approaches have been demonstrated individually. The next step, demonstrated in this paper, is integrating the optical technologies into subsystems to create and implement multiple synchronous optical packet buffers.

In this paper, it is assumed that packets are of a fixed size as the buffer technology currently implemented has a single fixed sized delay loop. However, packets are of variable length in currently implemented Internet protocol (IP) networks. Synchronization to timeslots of the smallest packet size is advantageous when variable length packets of integer lengths are used as channel utilization is increased. Recent work has been demonstrated for variable length recirculating optical packet buffers and is the next step toward realizing optical buffers for variable sized packets [18].

A major challenge prior to this study for asynchronous optical packet switching is the ability to detect optical labels and payloads that were generated by independent transmission sources. Due to the nature of optical packet switching where packets are switched and multiplexed coarsely on the packet level, labels and payloads will be completely asynchronous on the bit-level [5]. This requires the development of asynchronous burst mode label and payload detectors, which are not commercially available.

Previously, asynchronous optical forwarding of labeled optical packets was demonstrated for high bit-rate variable length 40 Gb/s payloads based on lower bit-rate 10 Gb/s labels [3]. End-to-end asynchronous optical transmission, forwarding, and detection have been shown for Internet protocol (IP)

Manuscript received September 1, 2009; revised October 13, 2009; accepted October 24, 2009. Date of publication January 8, 2010; date of current version October 6, 2010. This work was supported by the Defense Advanced Research Projects Agency (DARPA)/Microsystems Technology Office (MTO) and Army Research Laboratory (ARL) under Label Switched Optical Router (LASOR) Award W911NF-04-9-0001.

J. P. Mack, J. M. Garcia, H. N. Poulsen, B. Stamenic, G. Kurczveil, K. N. Nguyen, K. Hollar, J. E. Bowers, and D. J. Blumenthal are with the Electrical and Computer Engineering Department, University of California, Santa Barbara, CA 93106 USA (e-mail: jmack@ece.ucsb.edu).

E. F. Burmeister was with the Electrical and Computer Engineering Department, University of California, Santa Barbara, CA 93106 USA. She is now with Ciena Corporation, Linthicum, MD 21090 USA.

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Digital Object Identifier 10.1109/JSTQE.2009.2035712

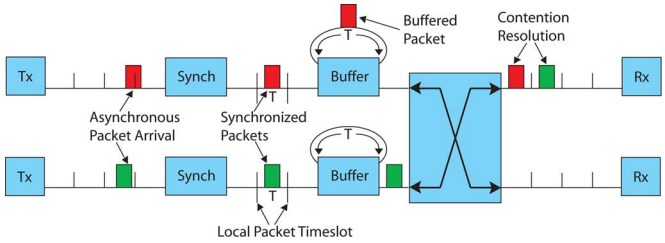

Fig. 1. Synchronous buffers align packets to local packet timeslots and resolve contention. (Tx: transmitter, Rx: receiver.)

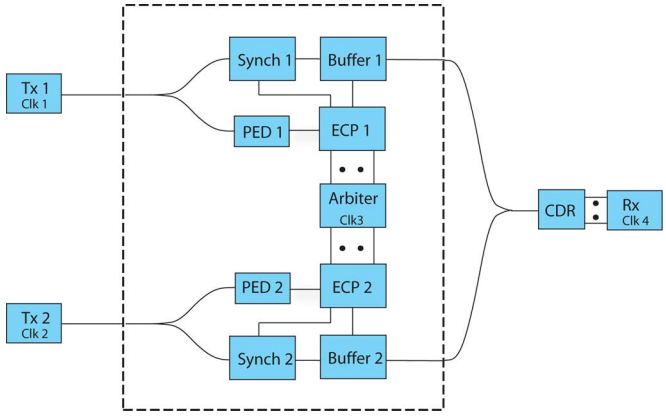

Fig. 2. Experimental setup for asynchronous contention resolution using multiple transmitters, synchronizers, and buffers. (PED: payload envelope detector, ECP: electronic channel processor, CDR: clock and data recovery.)

packets adapted to a labeled optical packet format for 12.5 Gb/s payloads with 3.125 Gb/s labels [20]. Asynchronous transmission, buffering, forwarding, and detection of 160 Gb/s payloads based on all-optical label processing has also been demonstrated [21]. In all of the previous work, contention of optical packets was preengineered using a single transmitter. In this paper, asynchronous time division multiplexing of packets generated from multiple independent sources is demonstrated using synchronous optical packet buffers.

First, the concept of synchronous buffering of fixed sized optical packets is presented. Second, the architecture and subsystems for asynchronous optical packet synchronization and buffering are discussed. This includes easily reconfigurable field programmable gate array (FPGA) based transmitters operating on independent and asynchronous clocks. The optical synchronizer and buffer designs used in this work are presented, which are based on semiconductor optical amplifier (SOA) switches and fiber delay lines. A burst mode FPGA-based receiver is presented that is capable of detecting asynchronous 10 Gb/s optical packets. Third, asynchronous optical packet synchronization, buffering, and time division multiplexing of packets generated from independent sources is demonstrated and performance measurements are presented. Finally, the power consumed by the synchronous optical packet buffers is presented and future power reduction possibilities are discussed.

II. Synchronous Optical Packet Buffer Concept

The challenge of asynchronous packet arrival and contention resolution is illustrated in Fig. 1. Packets arrive asynchronously at the inputs of optical switches due to clock and packet level uncertainties. In order to efficiently buffer and forward asynchronous packets, incoming packets must be aligned to the packet timeslots of the switch through the use of synchronizers. Packets are then synchronously loaded into and unloaded from buffers to resolve temporal collisions of packets contending for the same output port. Synchronous buffering is a critical component of any router as synchronization guarantees minimal uncertainty of the location of packets within buffers and allows for efficient time division multiplexing of packets onto output ports. Overall control logic complexity is reduced through the use of synchronizers as all buffering decisions can be made on a timeslot scale not at the clock scale. Synchronization at the input ports of optical packet switches leads to flexibility as both input and output buffer queuing can be implemented. Furthermore, only packet-level synchronization with a resolution of a clock cycle is required, as burst mode receivers are used to recover data on a per packet basis; therefore, bit-level synchronization is not necessary.

III. Architecture and Subsystems

A. Setup and Electronic Lookup

The schematic for asynchronous time division multiplexing of optical packets is depicted in Fig. 2. Multiple independent transmitters are used to generate optical packets that are asynchronous to each other, the electronic lookup, and the optical buffers. To demonstrate this technique, it is assumed that incoming packets are all destined for the same output port and labels are not utilized. The electronic lookup consists of payload envelope detectors (PEDs), FPGA-based electronic channel processors (ECPs), and an FPGA-based arbiter [22]. The ECPs and arbiter operate on the same clock, which is 156.25 MHz equivalent to 6.4 ns. The arbiter generates a local timeslot counter with clock cycles of 6.4 ns and duration of 64 ns, equivalent to 10 clock cycles. The fixed size timeslots are used to determine all routing decisions.

Asynchronous optical packets enter the switch fabric and the envelopes are extracted using the PEDs, which provide a precise time reference of the rising and falling edges of the packets. The envelopes are clocked into the electronic lookup time domain using D flip-flops in the ECPs. The ECPs then forward the payload envelopes to the arbiter for synchronization, contention resolution, buffer management, and forwarding lookup. The rising edge of the envelope is found and compared to the current count of the timeslot counter. Based on the count, the number of clock cycles needed to delay the rising edge of the packet to the next timeslot is determined. The arbiter generates SOA gating signals to select the delay of the optical synchronizer in order to align incoming optical packets to the local timeslots. The envelopes are then synchronized to the beginning count of the next timeslot and expanded to 64 ns. Since the incoming asynchronous optical packets are synchronized to the timeslot, all buffering and routing decisions can now be made on the

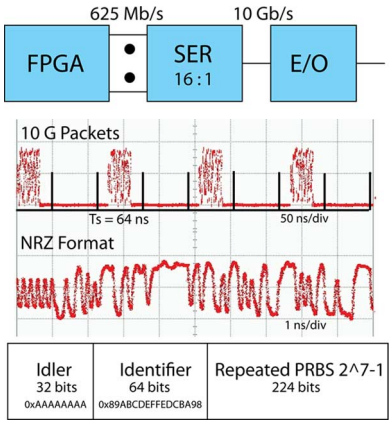

Fig. 3. FPGA-based transmitter screen shots of 10 Gb/s packet stream, NRZ format, and packet structure. (Ser: serializer.)

timeslot scale, which greatly simplifies the logic needed and guarantees that packets can be switched and multiplexed efficiently. Next, the arbiter compares the synchronized expanded envelopes from the input ports to determine if contention is present. The arbiter uses a round robin approach to determine which packet from the incoming ports should be buffered. Here, it is assumed that the buffers will only have to either pass a packet through or circulate a packet for one timeslot. The arbiter generates SOA gating signals to latch packets in and out of the buffers. The synchronized and buffered packets from both ports are coupled together for time division multiplexing. Finally, the asynchronously synchronized and buffered packets are detected by a burst mode clock and data recovery (CDR) circuit and an FPGA-based error analyzer.

B. Asynchronous Optical Packet Transmitters

The transmitters used are FPGA-based running on a 625 MHz local clock that is internally divided down to a 156.25 MHz clock for the main processing, as shown in Fig. 3. Packet streams are generated using software on a PC and loaded into 64 bit registers in the FPGA through a USB interface. The 64 bit wide registers are multiplexed from 156.25 Mb/s to 16 channels at 625 Mb/s in the FPGA. The data is further multiplexed to a single serial 10 Gb/s line using an external 16:1 serializer (Ser) circuit. The data stream is then converted to the optical domain using a continuous wave (CW) laser source, 10 GHz electro-optic modulator, erbium doped fiber amplifier (EDFA), bandpass filter (BPF), and a variable optical attenuator (VOA). In the following experiments, the transmitters are loaded with the same packet stream that consists of a 40-B nonreturn-to-zero (NRZ) packet at 10 Gb/s with a total period of 128 ns, as shown in Fig. 3. The 40-B packets contain a 32-bit idler, 64-bit unique packet identifier, and repeated 2^7–1 pseudo random bit sequence (PRBS). The idler was used to provide ample time for burst mode clock recovery. The fixed timeslots used in the following experiments are 64 ns that consist of a 40-B packet and 32 ns of guard band. The guard band was chosen to give ample room for timing uncertainties and switching speeds.

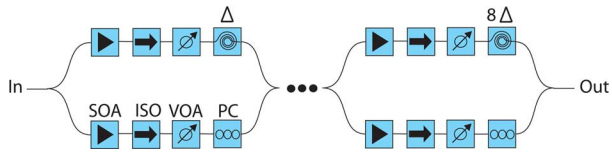

Fig. 4. Fiber-based feed-forward four-stage optical synchronizer with SOA gates. (ISO: isolator, VOA: attenuator, PC: polarization controller.)

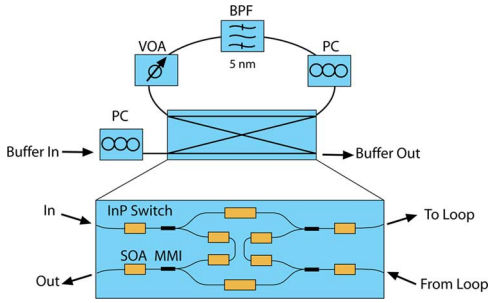

Fig. 5. Feedback recirculating optical buffer based on a packaged 2 × 2 InP switch matrix with fiber delay line. (VOA: attenuator, PC: polarization controller, BPF: bandpass filter, MMI: multimode interference coupler.)

C. Optical Packet Synchronizer

The demonstrated synchronizer is based on a feed-forward binary design that utilizes bulk SOAs and fiber delay lines as shown in Fig. 4. A four-stage synchronizer was chosen to provide a small enough resolution to match the period of the local clock, equivalent to 6.4 ns. The relative delay through any configuration of the synchronizer can be given as $T(n) = n \times \Delta$ ($n = 1, 1, 2, \ldots, 16$), where $\Delta = 6.4$ and the maximum delay tuning range is 102.4 ns. A combination of SOAs was used as the gates to select the delay and compensate for losses. The attenuators were tuned so that the insertion losses for the various paths were as close as possible with less than 2 dB maximum difference. A BPF with a bandwidth of 2.4 nm was placed after the synchronizer to remove out of band amplified spontaneous emission (ASE). The delay tuning range was chosen to match the size of the buffer or period of the local timeslots, equivalent to a period of 64 ns. Here, only 10 of the 16 delays are used to align packets to the local timeslots, equivalent to 64 ns. The synchronizer has been shown to dynamically synchronize fixed and variable length packets at 40 Gb/s with minimal power penalties [6], [23].

D. Optical Packet Buffer

The buffer combines a packaged integrated 2 × 2 InP based switch matrix with a fiber delay line to create a recirculating loop optical buffer, as illustrated in Fig. 5. The integrated switch matrix has low crosstalk (<–40 dB), high extinction ratios (>40 dB), fast switching (<1 ns), and can operate up to 40 Gb/s [24]. Here, packets can either pass through the buffer or circulate inside the fiber loop based on the gating of SOAs. The fiber loop delay is the same duration as the timeslot, equivalent to 64 ns. Furthermore, the 2 × 2 InP switch matrix is fabricated on a standard offset quantum well platform. The benefits of this

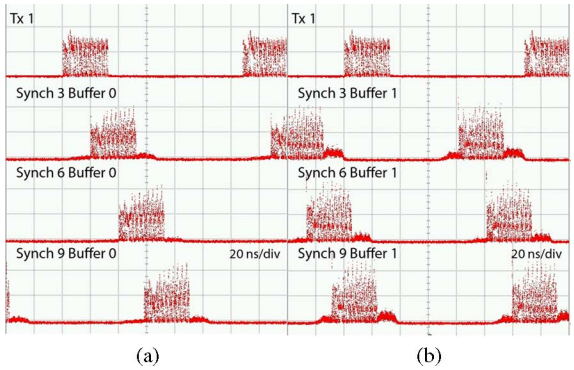

Fig. 6. Screenshots of transmitted, synchronized, and buffered packets (a) Synchronizer delays $n = 3$, 6, and 9 and buffer delay $n = 0$. (b) Synchronizer delays $n = 3$, 6, and 9 and buffer delay $n = 1$.

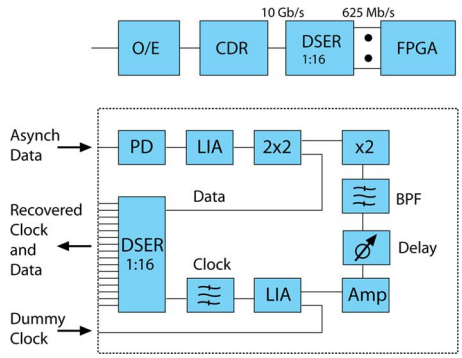

Fig. 7. FPGA-based burst mode receiver with inset of clock and data recovery (CDR) circuit. (Dser: de-serializer, PD: photodetector, LIA: limiting amplifier, BPF: bandpass filter.)

platform include ease of fabrication, the possibility of future integration with other standard photonic integrated circuits, and linear performance at higher output powers due to the lower confinement factor [24]. Also, the amplifier directly before the delay is flared to further mitigate saturation effects [24]. The maximum hold time of the buffer for 40-B packets at 40 Gb/s has been reported to be ten circulations [25]. Multiple optical buffers have been shown to successfully resolve contention of 40 Gb/s payloads based on 10 Gb/s labels [26]. Screenshots were taken for different delay combinations of the synchronizer equivalent to 19.2, 38.4, and 57.6 ns ($n = 3$, 6, and 9) and buffer equivalent to 0 and 64 ns ($n = 0$ and 1), as shown in Fig. 6.

E. Asynchronous Burst Mode Receiver

The clock and data recovery (CDR) circuit and FPGA-based packet detector used in the following experiments are depicted in Fig. 7 [27]. The packet stream is converted to the electrical domain using a 10 GHz photo detector followed by a 10 GHz limiting amplifier (LIA). The recovered data is split using a 2×2 cross point switch where part of the data is fed through, and the other injected into a frequency doubler to convert the 5 GHz base bandwidth of the NRZ data to a 10 GHz signal. The doubled signal is then filtered using a narrow bandpass filter with a center frequency of 10 GHz and bandwidth of 400 MHz

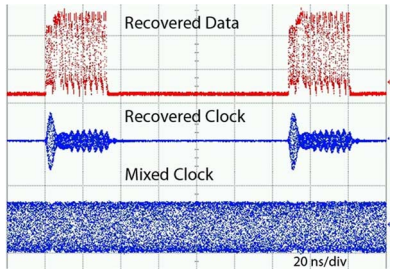

Fig. 8. Screenshots of recovered data from back-to- back with transmitter, recovered clock, and mixed clock.

that gives out a 10 GHz tone when data is present with 800 ps rise and fall times. The recovered clock travels through a tunable delay to finely align the recovered data and clock. The recovered clock is amplified and injected into the positive input of a 10 GHz differential LIA. Since the recovered clock is only present when data is present, an attenuated 10 GHz dummy clock derived from the receiver FPGA is injected into the negative input of the LIA. This insures that a clock is always present regardless if data is present. The dummy clock is attenuated so that when data is present the recovered clock gains dominance and only the recovered clock exits the output of the amplifier. When data is not present, the dummy local clock gains dominance and outputs from the amplifier. The mixed clock is filtered and the data is delayed to match the clock recovery circuit.

The recovered data, clock, and mixed clock of the transmitted signal are shown in Fig. 8 as an example of the CDR circuit operation. Both the recovered data and clock are used as inputs of a 1:16 deserializer (Dser) that converts the 10 Gb/s asynchronous data to 625 Mb/s parallel data channels and the recovered clock to 625 MHz. The recovered data and clock enter a receiver FPGA-based board operating on 625 MHz and divided 156.25 MHz clocks. The data is further demultiplexed down to 64-bit parallel channels from 625 to 156.25 Mb/s and the recovered clock is divided from 625 to 156.25 MHz. The FPGA implements a 64-bit wide by 512-bit deep asynchronous first in first out RAM block to transfer the recovered data to the local clock domain of the FPGA for performance analysis.

The receiver FPGA performs real-time packet analysis by looking for the 64-bit unique packet identifier within the recovered data. If a packet is identified successfully then the FPGA updates a counter of packets recovered. The counter is written into a register that is read through a USB interface using custom software. A GUI is used on a PC to display packet recovery in real-time and also to change the capture length and expected packet recovery on-the-fly. The recovered counter is compared to the expected number of packets received to obtain a real-time packet recovery measurement. For the following experiments, each measurement expected 10 000 packets and was averaged over five measurements, so a total of 50 000 packets were expected for each data point.

It is important to note that a typical bit –error rate (BER) measurement cannot be conducted for the following experiments because the packet arrival is random and asynchronous. It is assumed that when a packet is lost, either a single bit, multiple

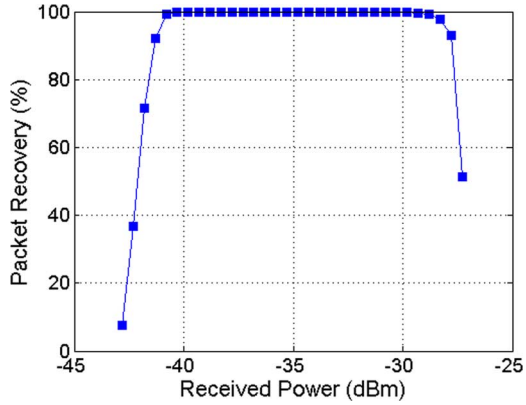

Fig. 9. Packet recovery measurement for a typical asynchronous back-to-back experiment.

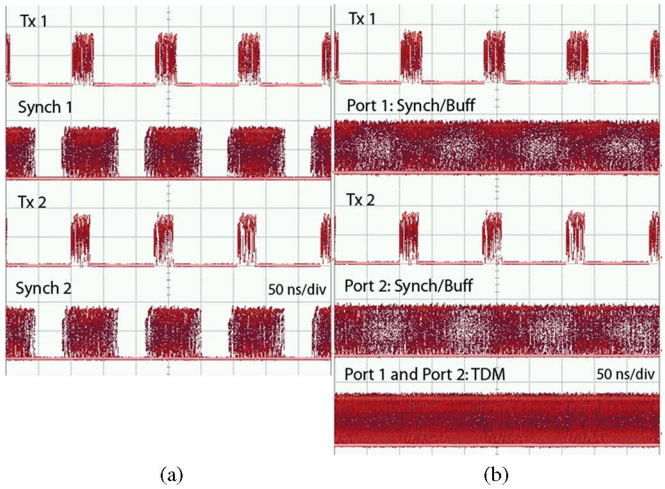

Fig. 10. (a) Screenshots of transmitted packets and synchronized packets from both ports. (b) Screenshots of transmitted packets, synchronized and buffered packets from both ports, and time division multiplexed packets. (Tx: transmitter, TDM: time division multiplexed.)

bits, or all 64 bits of the identifier are corrupted. Furthermore, the expected count is generated in the receiver for simplicity, which leads to fluctuations in packet counts because the transmitter and receiver operate on asynchronous clocks. The current packet loss sensitivity is 10^{-5} and can be increased in the future by proper triggering of the transmitter and receiver.

Packet recovery measurements were conducted for an asynchronous back-to-back experiment and are depicted in Fig. 9. Packet recovery $>$99.99% was achieved for a dynamic range of received powers $>$10 dB. For received powers less than -41 dB·m, the number of packets recovered decreases as the SNR becomes too low for the signal to be recovered properly. For high received powers >-29 dB·m, the photo detector and limiting amplifier in the receiver become saturated, which distorts the incoming signal and lowers the number of packets received. Achieving a large dynamic range of input powers is critical when capturing packets from an asynchronous optical packet system where many states are exercised randomly that have different insertion losses, noise accumulation, and extinction degradation. In order to achieve high performance, when using many input ports with multiple synchronizer and buffer states, the dynamic range of the different states must overlap. Furthermore, the dynamic range of the time division multiplexed (TDM) outputs will be reduced as the relative difference and offset of dynamic range for each state increases.

IV. Asynchronous Optical Packet Synchronization and Buffering

The experimental setup used to demonstrate asynchronous contention resolution with multiple input ports where packets are synchronously loaded into optical buffers is shown in Fig. 2. Incoming asynchronous packets are dynamically aligned to the local timeslot on a per packet basis using optical synchronizers. How often the delay/state of the synchronizer changes is based on the frequency difference of the clocks in the transmitter and arbiter. As the frequency of the clocks drift apart the rising edge of the packets drift across the timeslot and the delay needed changes. Once the packets are synchronized, they are loaded into and unloaded from the buffers, and buffering decisions are made on a timeslot scale. The arbiter uses a round robin approach to buffering where the buffers alternate circulations when contention is present. Packets from both buffers are efficiently TDM on a timeslot scale and detected by the asynchronous receiver.

Screenshots were taken for the outputs of both synchronizers operating asynchronously and are shown in Fig. 10(a). Here, the oscilloscope was triggered for packets from the output of each synchronizer by their respective transmitter. The oscilloscope settings were changed to an eye mask mode where data is displayed concurrently over several seconds so the location of the packets can be seen. The packets from the transmitters appear in a single location, as the scope is triggered on the period of the transmitted signal. As is expected, the packets from the synchronizer output appear blurred. What appears on the scope is essentially an overlap of all the randomly changing delays/states of the synchronizer. Packets entering the synchronizer are dynamically aligned to the timeslot, which is 64 ns, but the timeslot and the trigger from the transmitter are asynchronous to one another. The delay a packet undergoes when passing through synchronizer under asynchronous operation is between 6.4 and 64 ns, which is essentially random. Therefore, the packets are blurred across the timeslot, as can be seen in the screenshots.

Packet recovery measurements were conducted for each asynchronously operating synchronizer separately, shown in Fig. 11. There is an offset in the back-to-back curves of the two transmitters because the modulator bias of each transmitter was adjusted separately to obtain the largest dynamic range possible. Greater than 99.99% packet recovery was obtained for a range of received powers $>$5 dB for both asynchronously operating synchronizers. The dynamic range of packet recovery after synchronization is reduced because the packets are gated, which affects the operation of the LIA in the receiver. Negative power penalties were obtained likely due to the gating of packets using SOAs that have a higher extinction compared to the

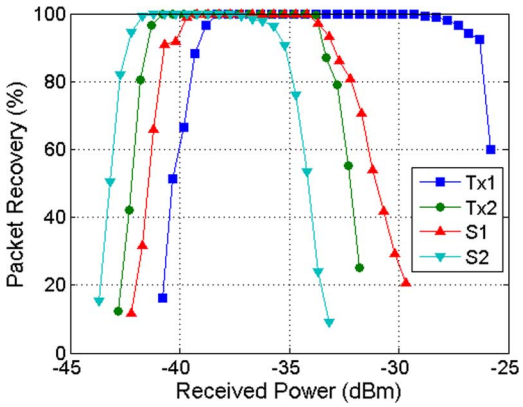

Fig. 11. Packet recovery measurements for the transmitters and asynchronously operating synchronizers. (Tx: transmitter, S: synchronizer.)

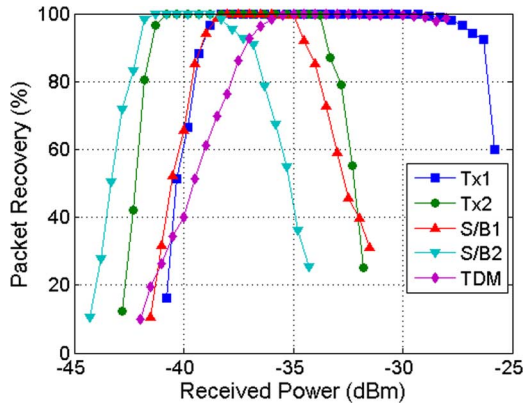

Fig. 12. Packet recovery measurements for the asynchronous transmitters, the synchronized and buffered packets from ports 1 and 2 and the time division multiplexed packets from both ports. (Tx: transmitter, S/B: synchronizer and buffer, TDM: time division multiplexed.)

transmitter, and through the use of a pre-amplified receiver that operates on average power.

Contention resolution of asynchronous packets using multiple synchronizers and buffers was also demonstrated. Here, packets from both asynchronous inputs are synchronized to the arbiter timeslot on a per packet basis and loaded into the buffers. The arbiter alternates buffering on each port when contention is present. Since the transmitters operate on independent clocks, sometimes packets from the two ports will occupy the same timeslot so a packet must be buffered, and sometimes they occupy different timeslots so they pass through the buffers. Again, how often the state changes from when buffering is needed and when it is not is related to the frequency drift of the two transmitters. Screenshots were taken of the synchronized and buffered packets for both ports separately and the combined TDM packets from both ports, as shown in Fig. 10(b). The signal appears completely blurred across the screen, which is expected. The arbiter timeslot is asynchronous, and the transmitters are asynchronous to one another, so first, the packets are blurred across the timeslot due to synchronization, and second, sometimes packets are buffered and sometimes not, so the two timeslots are filled with packets randomly. The TDM packets from the two ports appear completely blurred as well, and the only way to verify that packets are being multiplexed correctly is to analyze the bits within the packets.

Packet recovery measurements were taken for the two ports separately and for the TDM from the two ports, as shown in Fig. 12. Each port experiences 20 different states, and 40 different states when combined. Packets not only experience different insertion losses, but now experience different SNR degradations and pattern dependence. This is due to the increased number of cascaded SOAs for buffered packets compared to nonbuffered packets. Nonetheless, greater than 99.9% packet recovery measurements with minimal power penalties were obtained for the asynchronously operating synchronizers and buffers for both ports with a range of operation >4 dB. Variable optical attenuators were used at the outputs of the two ports to obtain optimal operation into the receiver for both ports separately, then the signals were combined to generate TDM packets and analyzed. Greater than 99.9% packet recovery was obtained for a range of received powers >5 dB for the TDM packets. Here, the curve shits by approximately 3 dB as the number of packets is doubled. The slope also changes and could be due to the difference in modulator bias, which affects the extinction of the packets from the two ports. Also, the range of operation increases probably due to the LIA being designed to handle continuous, not bursty, data, and the combined signal has more bits. This verifies the first demonstration of asynchronous optical packet synchronization and buffering where asynchronous packets are TDM to avoid temporal collisions based on a local timeslot.

V. Power Consumption

The power consumed by the synchronizers and buffers were measured. For the top port, the power consumed by the synchronizer and buffer was 8.2 and 7.7 W, respectively. It is important to note that the calculations include the power needed to drive the photonic devices as well as the power required to regulate the temperature of each device. Photonics are highly temperature dependent, so temperature controllers are required for proper operation. Furthermore, the photonic devices require electronic drivers to make the devices operational, so the power consumed in the drivers must go hand in hand with the power consumed in the optics. In order to further investigate where the majority of power is consumed in the optical technologies, power estimates were calculated for the synchronizer and buffer. Packaged components were used that had the optical devices, electronic drivers, and temperature controllers powered by a common power supply. The power consumption of the optical devices can only be estimated by assuming that the powers consumed were at maximum biasing of the SOAs, and the rest was consumed by electronic power dissipation and temperature control, which were estimated from data sheets. The results for the estimated breakdown of power consumed in the synchronizer and buffer are depicted in Figs. 13 and 14. A majority of the power in the synchronizer and buffer is not consumed in the photonics, but rather in the electronic drivers and temperature controllers.

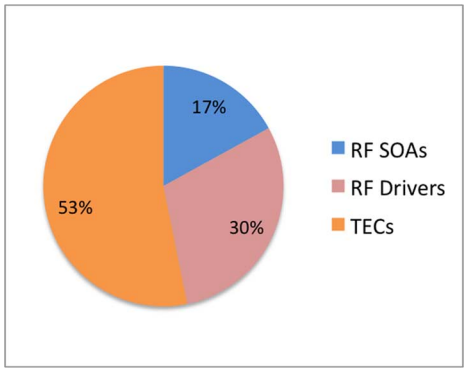

Fig. 13. Estimated power breakdown of the optical synchronizer. (TEC: thermoelectric cooler.)

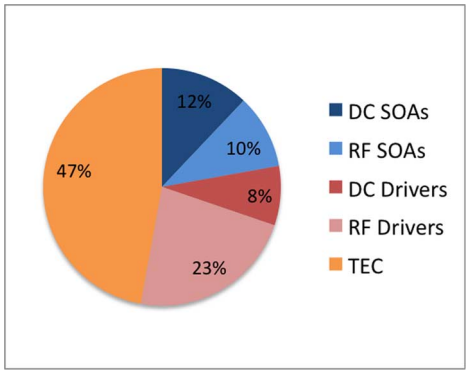

Fig. 14. Estimated power breakdown of the optical buffer. (TEC: thermoelectric cooler.)

The majority of power consumed in the photonic devices by themselves was dissipated by the SOAs used for the synchronizers and buffers. All of the photonic devices required SOAs for switching as well as to compensate for losses due to coupling, splitting, and propagation. If these losses can be reduced, then fewer and smaller SOAs can be used, which would reduce power. Electronic drivers are a necessity for operating photonic devices and cannot be neglected; however, using electronics that dissipate lower power will result in an overall power reduction. Most photonic devices are currently highly temperature dependent, so temperature regulation is required, which consumes the majority of power. If alternative means of temperature control that draw less power are implemented or temperature independent photonics are used, then the power consumed by the photonic devices can be reduced drastically. It should be noted that although the use of synchronous buffers increases total power consumption compared to architectures that do not implement synchronization, overall control logic complexity is reduced that may reduce electronic power consumption. Although, it is too early in the development of optical buffers to directly compare the power consumption of the demonstrated synchronous optical packet buffers to commercially implemented RAM in electronic routers, the power consumption can be used as a benchmark for future optical buffering technologies.

VI. Summary and Conclusion

The first demonstrations of asynchronous time division multiplexing of optical packets using multiple synchronous optical buffers have been presented. Asynchronous optical packet transmitters and receivers were developed as a means of measuring performance of the synchronous optical buffers. In this paper, greater than 99.9% packet recovery was achieved for an asynchronously multiplexed packet stream generated from multiple independent transmitters. The demonstrated synchronous buffers can reach 40 Gb/s and beyond with no change to the photonic devices, firmware, or power consumption.

There are several limitations in the synchronous optical packet buffers that must be overcome in order to be practical. There are physical layer limitations that include polarization dependent loss, insertion loss, accumulated noise, pattern dependence, and extinction ratio degradations. Although photonic integrated technologies were used, all the optical technologies implemented must be integrated in order to reduce timing uncertainties, latency, and footprint. The optical buffer architecture must be enhanced to operate with variable length packets. The statistical significance of the packet recovery measurements must be increased to demonstrate its use in practical applications. The power consumed by the synchronous buffers must be reduced using efficient SOAs, current drivers, and temperature controllers.

Acknowledgment

The authors would like to thank G. Epps from Cisco Systems for helpful discussions.

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John P. Mack received the B.S. degree in electrical engineering from Columbia University, New York, NY, in 2004 and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of California, Santa Barbara, in 2005 and 2009, respectively.

He is currently with the Electrical and Computer Engineering Department, University of California. His research interests include optical packet switching, asynchronous optical communications, and FPGA-based prototyping. His recent research efforts are focused on developing asynchronous optical packet routers that use InP-based photonic integrated technologies.

Emily F. Burmeister received the B.S.E. degree in engineering physics from the University of Michigan, Ann Arbor, in 2002 and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of California, Santa Barbara, in 2004 and 2008, respectively.

She is currently with Ciena Corporation, Linthicum, MD.

John M. Garcia received the B.S. degree in computer science from the University of California, Santa Barbara, in 2007. He is currently working toward the Ph.D. degree in electrical and computer engineering in the Electrical and Computer Engineering Department, University of California, with a focus in electronics and photonics.

His current research interests include optical networks, optical packet switching, and optical packet routing.

Henrik N. Poulsen was born in Copenhagen, Denmark, in 1969. He received the M.Sc.E.E. degree from the Technical University of Denmark, Copenhagen, in 1995.

He is currently with the Electrical and Computer Engineering Department, University of California, Santa Barbara. His research interests include multi-wavelength all optical packet switching including the interface between low-speed electronic control planes and high speed all-optical planes.

Biljana Stamenic, photograph and biography not available at time of publication.

Geza Kurczveil received the B.S. degree in physics from the University of California, Santa Cruz, in 2006 and the M.S. degree in electrical engineering from the University of California, Santa Barbara, in 2009. He is currently working toward the Ph.D. degree in electrical and computer engineering in the Electrical and Computer Engineering Department, University of California, Santa Barbara.

His current research interests include integrated optical buffers with regenerators and low-loss Silicon waveguides.

Kimchau N. Nguyen received the B.S. and M.Eng. degrees in electrical engineering from the University of Louisville, Louisville, KY, in 2005 and 2007, respectively. She is currently working toward the Ph.D. degree in the Electrical and Computer Engineering Department, University of California, Santa Barbara.

Her current research interests include photonic integrated circuits, high-speed optoelectronic devices, and coherent optical communications.

Kurtis Hollar received the B.S. degree in electrical engineering from the University of California, Santa Barbara, in June 2007. He is currently working toward the M.S. degree in electrical and computer engineering in the Electrical and Computer Engineering Department, University of California.

His current research interests include optical networks, high-frequency solid state electronics, technology management, and renewable energies.

John E. Bowers (F'04) received the M.S. and Ph.D. degrees from Stanford University, Stanford, CA.

He is the Fred Kavli Chair in Nanotechnology, the Director of the Institute for Energy Efficiency, and is currently a Professor in the Electrical and Computer Engineering Department, University of California, Santa Barbara. He was with AT&T Bell Laboratories and Honeywell before joining University of California. He is the cofounder of the Center for Entrepreneurship and Engineering Management (now the Technology Management Program), Calient Networks, and Aurrion. He is the author or coauthor of more than eight book chapters, 450 journal papers, 700 conference papers and has received 52 patents. His research interests include the development of novel optoelectronic devices for the next generation of optical networks.

Dr. Bowers is a member of the National Academy of Engineering, a fellow of the OSA and the American Physical Society, and a recipient of the OSA Holonyak Prize, the IEEE LEOS William Streifer Award and the South Coast Business and Technology Entrepreneur of the Year Award. He and coworkers received the ACE Award for Most Promising Technology for the hybrid silicon laser in 2007.

Daniel J. Blumenthal (S'91–M'93–SM'97–F'03) received the B.S.E.E. degree from the University of Rochester, Rochester, NY, in 1981, the M.S.E.E. degree from Columbia University, New York, in 1988, and the Ph.D. degree from the University of Colorado, Boulder, in 1993.

He is currently a Professor in the Electrical and Computer Engineering Department, University of California, Santa Barbara (UCSB). He is also Director of the LASOR center at UCSB, a project funded by the DARPA/MTO Data in the optical domain network program. He is a cofounder of Calient Networks (established 1999) and more recently Packet Photonics, LLC. His research interests include optical communications, photonic packet switching and all-optical networks, all-optical wavelength conversion and regeneration, ultrafast communications, InP photonic integrated circuits, and nanophotonic device technologies. He is the author or coauthored of more than 300 papers in these and related areas and holds 7 patents.

Dr. Blumenthal is a fellow of the LEOS and Communications Societies) and fellow of the Optical Society of America. He is recipient of a 1999 Presidential Early Career Award for Scientists and Engineers from the White House, a 1994 National Science Foundation Young Investigator Award, and a 1997 Office of Naval Research Young Investigator Program Award.