An Adaptation Layer for Real-Time Interoperability Between Legacy 100MbE and 40Gb/s (and Beyond) Optical Label Switched Networks

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Abstract: We present a method, scalable to 1Tb/s transmission systems, of performing electronic lookup on asynchronous 40Gb/s burst mode channels to facilitate real-time end-to-end interoperability between legacy 100MbE networks and 40Gb/s optical label switched networks.

Introduction

Data switching requirements are projected to reach the order of a Petabit per second (Pbps) in the near future [1]. This rapid increase of network bandwidth has sparked industry interest for commencing 1TbE initiatives shortly after 100GbE is standardized [2]. Optical packet switching (OPS) and single-channel 1Tb/s transmission systems are under investigation as possible solutions that can scale efficiently with bandwidth in terms of power and footprint [3-4]. As 1TbE technologies become deployable, adaptation layers will be required for real-time interoperability between all-optical networks and legacy network architectures.

The bulk of the Terabit transmission systems investigated to date can be generalized into setups that consist of narrow pulse sources (<1ps) followed by amplitude and/or phase encoders, and an M-order optical time division multiplexing (OTDM) stage. Conversely, a receiver can consist of an optical de-multiplexion stage based on optical gating followed by $N \leq M$ optical demodulators. In all cases, bit error rate testers (BERT) or pattern generators are used as the encoding mechanisms of a transmitter and error analysis tools of a receiver, which rely on offline processing or one-at-a-time analysis of OTDM tributaries. Although an effort has been made to develop real-time transmitters and receivers for on-off keying (OOK) [5] and coherent systems[6, 7], there is still a need for a technology to enable proposed Tb/s transmission systems to dynamically generate and process data at ultra high bit rates. Achieving these dynamic functionalities will enable the deployment of such Tb/s transmission systems and facilitate their interoperability with current electronic networks.

In this paper we present an adaptation layer scheme, amenable to 1Tb/s scaling, to achieve end-to-end fully autonomous adaptation between commercial 100MbE networks and 40Gb/s optical label switched networks. Real-time assembly of 40Gb/s payloads is performed by means of electronic payload identifier recovery on deserialized streams that arrive out of sequence due to the asynchronous nature of having multiple free-running deserializers working in parallel.

Labeled Packet Format and Adaptation Layers

The optically labeled packet format assumed in this paper is illustrated in Fig. 1. It consists of a relatively low-speed (10Gb/s) optical header that can be processed electronically, in a manner that is energy efficient, by optical data routers (ODR) and a high-speed (40Gb/s and beyond) payload that is processed entirely in the optical domain. The optical header (OH) is made up of a 64-bit OH identifier (0x89ABCDEFFEDCBA98) that serves as a means of detecting OHs and a 10-bit label that is used by ODRs for routing purposes. The optical payload (OPL) is comprised of a 64-bit payload (PL) identifier (0x9BDFECA88ACEFDB9) that can be exploited in order to perform payload recovery and assembly within the clock domain of field programmable gate array (FPGA).

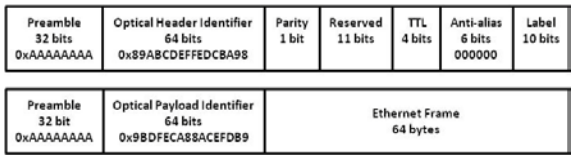

Fig.1: Optically labeled packet format: 10Gb/s NRZ optical header (top) and 40Gb/s RZ optical payload (bottom).

The adaptation layers are schematically shown in Fig. 2(a). Asynchronously arriving 100MbE frames enter the ingress FPGA where they are dynamically converted to optical labeled packets based on the destination IP address found in the IP header of each frame. Before the labeled packets are forwarded to the 40Gb/s serialization stages, they are split and internally serialized into four 16-bit 622Mb/s channels. The OH is repeated on all four channels so

that their serialization will result in a 10Gb/s OH. The OPL, on the other hand goes through two stages of encoding. First, bits (0, 4, 8 …) are sent through channel 0, bits (1, 5, 9 …) through channel 1, bits (2, 6, 10 …) through channel 2, and bits (3, 7, 11 …) through channel 3. This ensures that when the four output channels are serialized, the payload will be identical to its original form only compressed in time. Second, the Ethernet payload is 8b/10b encoded within each channel to ensure that the 64-bit payload identifier sequence does not occur within the payload.

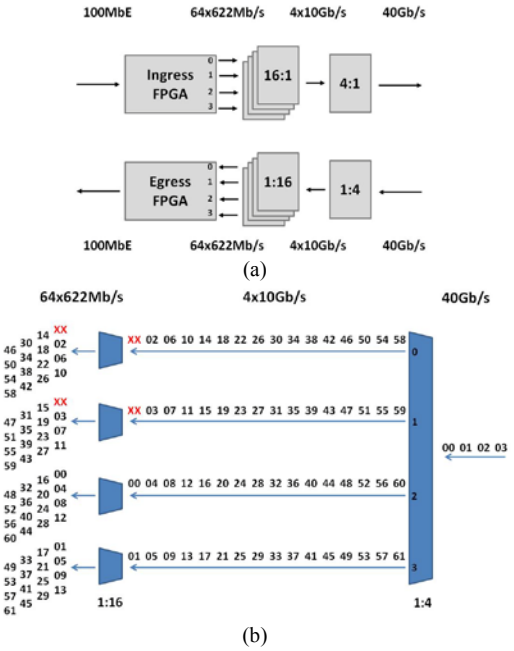

Fig. 2: (a) Adaptation between 100MbE frames and 40Gb/s optically labeled packets. (b) Non-ideal deserialization of a 40Gb/s serial stream.

At the adaptation egress, labeled packets are sent through the deserialization stages depicted in the bottom of Fig. 2(a) and are then converted to 100MbE frames that conform to the Ethernet standard. Data out of the deserialization stages will be divided into four 16-bit 622Mb/s channels in a fashion that is similar to the channel encoding used by the ingress adaptation layer. Ideally, the 40Gb/s data should arrive at the 1:4 deserializer and be split evenly between the 1:6 deserializers with bit 0 coming out of channel 0. Due to the nature of packets arriving asynchronous to the deserializer time slot, output data may be in a shifted sequence as illustrated by Fig. 2(b). The sequencing effect is only shown for the 1:4 deserializer, but it also occurs in the each of the 1:16 deserializers. The egress FPGA determines correct data sequencing by performing detection and recovery of the 64-bit PL identifier on each of the four 622Mb/s input channels. This is done by scanning each channel for one of four 16-bit identifiers (0xF497, 0x0FF0, 0x33CC, and 0x55AA) which correspond to the de-interleaving of the 64-bit PL identifier. Correct sequencing is determined when all four 16-bit identifiers are detected within one clock cycle of the FPGA local clock domain (6.4ns). Once sequencing is determined, the Ethernet payload is assembled and sent out through a 100BASE-TX Ethernet interface.

Results and Discussion

The scope traces rendered in Fig. 3 show the result of serializing the channel encoded payload (left column) and the result of serializing the repeated OH and channel encoded payload (right column). The signals out of the serialization stage are sufficient to drive a 40Gb/s OOK transmitter. To obtain the signals necessary for Tb/s transmission systems capable of assembling multiple asynchronous deserialized 40Gb/s channels into frame structures compatible with current transmission protocols such as Ethernet one need only duplicate the (de)serialization stages and slightly modify the channel encoding scheme.

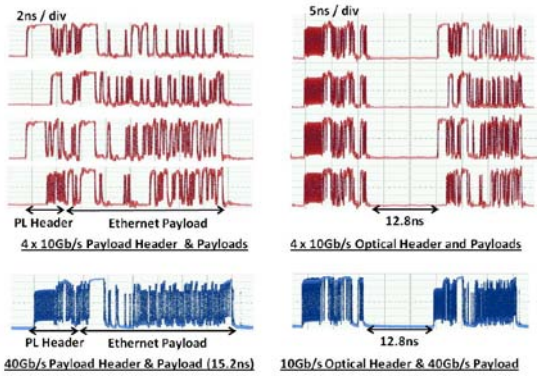

Fig. 3: Oscilloscope traces of the channel-encoded 10Gb/s optical header and 40Gb/s payload at each serialization stage.

The optical labeled packet format paired with the method to determine sequencing of asynchronous 40Gb/s deserialized channels presented in this paper serve as the foundations for a fully autonomous adaptation layer between 100MbE network layers and 40Gb/s (and beyond) optical label switched network layers.

3. Acknowledgement

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4. References

[1] J. Y. Hui, *IEEE GLOBECOM 2008*, ECP.484, 1-6, 2008.
[2] D. C. Lee, Proc. OFC'08, OThB.
[3] S. J. Ben Yoo, *JLT,* **24**, 4468-4492.
[4] C. Schmidth-Langhorst *et al*, Proc. OFC'09, OTuN5.
[5] J. P. Mack *et al*, Proc. OFC'10, OThN1.
[6] T. Omiya *et al*, Proc. OFC'11, OTuN3.
[7] T. Pfau *et al*, Proc. OFC'11, OTuN4.