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ABSTRACT

In this paper we present the rationale behind photonic integration of optical buffers for packet switching using optical delay lines. Our work on integrated buffers consisting of Indium-Phosphide-based gate matrix switches and silica-based delay lines is reviewed. Successful implementation of this hybridly integrated chip in a synchronously loaded optical packet buffer is shown. Integration of an optical buffer on the hybrid silicon platform, where active switches can be combined with a low-loss silicon delay line, is discussed and the results for a fully integrated 1.1-ns delay buffer are presented. We report on our current efforts to reduce the silicon waveguide loss to scale the hybrid silicon buffer to be able to store 40-byte packets.

Keywords: Optical buffers, optical memories, optical switches, photonic integrated circuits, semiconductor optical amplifiers (SOAs), hybrid silicon platform

1. INTRODUCTION

All-optical routers have the potential to offer greater bit-rate transparency and protocol flexibility than electrical routers while reducing power consumption [1]. One proposed solution toward realizing these goals is optical packet switching (OPS), which provides an efficient use of bandwidth by multiplexing data packets in time as well as wavelength and is the solution closest to the current Internet Protocol (IP) [2]. However, a remaining challenge in OPS is to resolve contention between packets competing for router resources. In electrical routers packets may be stored indefinitely in RAM. To avoid dropping packets or adding unnecessary latency in optical routers, optical memory, or buffering, is needed.

Previously, there has not been an optical buffering solution that is compact, scalable, and operates with data at high bit rates [3]. Optical memory technology must be able to buffer data from practical packet streams; this includes packet lengths of at least 40 bytes at bit rates of 40 Gb/s and higher with guard bands no more than several nanoseconds in length. At the same time, there are additional considerations such as cost, power consumption, and footprint that would limit the possible success of the technology. Delay line buffers dominate the proposed buffering approaches and have demonstrated successful buffering [4,5,6], but would offer more promise as a commercial memory element as an integrated technology. Integration has been shown to offer benefits such as lower cost, improved performance and better reliability [7]. Slow light buffers are interesting in the push to reduce footprint [8,9], but have fundamental limitations, largely in the form of a bandwidth-delay limit [10].

In this paper we first present the rationale behind photonic integration of optical buffers for packet switching using optical delay lines in section 2. Optical buffers in a recirculating, or feedback, configuration are shown to meet all requirements for 40-Gb/s operation with reasonable packet payload lengths, unlike alternative approaches based on e.g. slow light. In section 3 we demonstrate the first optical buffering of 40-byte packets of 40 Gb/s data using an on-chip optical buffer. The device consists of an InP-based, fast 2×2 switch and a silicon oxynitride waveguide delay. In section 4 we describe the realization of the first fully integrated optical buffer, fabricated in the hybrid silicon platform. The buffer has a delay of 1.1 ns, limited by the silicon delay line losses. Our current efforts to scale the fully integrated hybrid silicon buffers to 40-byte operation are summarized in section 5.
2. RATIONALE FOR RECIRCULATING OPTICAL BUFFER APPROACH

2.1 Optical packet switch architecture

Optical switching may become useful for data routing in the core of the network, leaving electrical routers for more intense processing at the edge of the network. Label switching is used to allow the data payload to remain in the optical domain while an electrical data processor reads the address information and makes the routing decisions. An example of a basic optical data router for optical packet switching is shown in Fig. 1. This design is the basis of the LASOR project and features buffering for asynchronous, labeled 40 Gb/s packets. The entire switch is described in detail in [11]. The system without synchronization or buffering was demonstrated using monolithic packet forwarding chips (PFCs). However, without buffers placed before the PFCs, packets must be managed a priori to avoid contention. This section presents a comparison of buffering approaches.

![Fig. 1 Schematic of an optical data router comprised of synchronizers (Sync), buffers, packet forwarding chips (PFC), packet envelope detectors (PED), clock data recovery (CDR), deserializers (Deser), an arrayed waveguide grating router (AWGR), and control electronics.][12]

2.2 Buffering requirements

Current routers use large capacities of electrical RAM to resolve contention. The state-of-the-art Cisco CRS-1 core router is based on linecards that operate with 2 GB of memory. This capacity is currently not feasible with any proposed optical buffering approach, but recent research has shown that much smaller buffering capacities are adequate. Simulations show that if access links are slower than the backbone network and the traffic is smoothed, then only ten packet buffers per output port are needed for 80% throughput [13]. Thus, optical buffers may present a realistic solution. Optical buffers must meet certain requirements to achieve acceptance. It is first necessary that a buffering approach can impart a delay of at least the length of the packet payload in order to provide contention resolution. It is important for the buffering device to be bit rate scalable to 10 Gb/s or greater to offer an advantage over electrical domain counterparts. For acceptable network loads, they should have the capability to store packets of no less than 40 bytes with guard bands no more than several nanoseconds long. Packet payload length is one of the more difficult challenges for many buffering approaches, but unless the ratio of the payload length to the overhead of the header and guardbands is reasonable, optical buffers and packet switches will not afford an advantage. In addition, it is desirable to require less header processing for a given amount of payload. In order to accommodate short guard bands, buffers must be able to switch or reset in less than several nanoseconds. Along with the above requirements, there are also other considerations that increase the probability of success of a given optical buffer approach. As usual, low cost is a main issue. Optical packet switches must lower the cost per bit for data transmission to make them advantageous. It is also necessary that optical buffers have low power consumption, low heat production, and a small footprint—the main challenges facing the scalability of electrical packet switches. For both cost and footprint, it is obviously important that the number and complexity of components included in a given buffer architecture must be kept to a minimum. In order to make the optical buffer more flexible, it is desirable for the buffer to be transparent to packet length and to provide dynamically variable storage time. Apart from these architectural considerations, it is also desirable that the buffer device impart the least possible dispersion and optical power penalty.

2.3 Buffering approaches

We review the advantages and limitations of two types of transparent optical buffering approaches and one approach based on the electrical conversion of packets. Transparent optical buffering approaches rely on delaying packets by increasing total transmission time, either by decreasing the group velocity (slow light buffers), or increasing the physical length (delay line buffers). Slow light buffers can be divided into two types; devices using material-based resonances...
and those using coupled resonant structures (CRS). Delay line buffers are also categorized into two subsets; feedforward and feedback. Slowing mechanisms proposed for optical buffers use strong resonances between electromagnetic waves (CRS) or between an electromagnetic field and a polarizable medium (material-based). In CRS such as gratings and photonic crystal defects, the group velocity is reduced by lengthening the light path through repeated reflections; the group velocity decreases drastically in the vicinity of the photonic bandgap. The band structure for polarizable media buffers looks very similar to that of the appropriate CRS dispersion curve with bandgaps created from strong material resonances. For the application of optical buffering, electromagnetically induced transparency (EIT) devices using resonances with exciton excitations in semiconductors are studied for their compactness. Population oscillation is an alternative material-based slow light technology similar to EIT. It utilizes a carrier population grating to create the material-based resonance. A more detailed overview of slow light buffer mechanisms can be found in [14,15]. Delay line buffers provide a practical solution and have demonstrated the best results. The two types are shown in Fig. 2. Data in a feedforward buffer is sent through a given delay line only once. The buffers must therefore use the same number of delay lines as the desired variation in delay times. Feedback buffers are operated to use the same delay line repeatedly. In a feedback buffer the length of the delay line determines the resolution of possible delays and in general should be made the length of the packet payload. The number of delay variations and maximum storage time are determined by the maximum number of recirculations.

![Fig. 2 Schematics of (a) feedforward and (b) feedback buffers](image)

### 2.4 Buffering comparisons

The three types of buffering approaches were studied to find the practical and theoretical limitations. This information is then used to contrast the advantages. Before comparing transparent optical buffers, it is necessary to consider the challenges in the electrical domain. Although speed appears to limit the scalability of electrical RAM, recent research shows that silicon-based CMOS RAM can be used as a storage medium for optical packets at data rates up to 40 Gb/s by using a combination of optical and electrical components [16]. Because bits are stored electronically, such a design offers very long storage times, large capacity, and random access at arbitrary times. However, loss and component complexity have limited the design to packets of less than 10 bytes [16]. The buffer uses serial to parallel conversion of packets, and therefore each packet must be split into the same number of streams as bits in the packet. The maximum amount of splitting, and therefore maximum number of bits is determined by the amount of power needed to accurately read the bits. The restriction on maximum packet size greatly limits the maximum load of the network. Slow light devices offer many desirable higher-level advantages, but the fundamental limitations that are outlined here will inhibit their use as buffers. Slow light buffers are heavily researched because they potentially offer a compact solution that has continuously variable storage times and can handle asynchronous packets of varying lengths. However, dispersion, bandwidth, and loss are fundamental issues that will limit the use of slow light devices as buffers. Slow light shows promising results if data rate and packet length are ignored. Fig. 3 shows the relative compactness and loss tradeoffs for variations on slow light compared to integrated feedback buffers. Electromagnetically induced transparency under extreme cooling (7 K) and ideal coupled resonators show the best results in this figure because of the large degree of slowing they impart. However, the three regions show a lot of overlap in terms of the degree of delay per loss, despite the very large effective group index of the slow light methods. This is due to very high losses which will end up being one of the limiting factors. The best slowing results were commonly obtained using optimized pulses in short devices.
In order to quantify the limitations for slow light buffers with given data rates and packet lengths, equations were presented relating the index, or degree of slowing, with these parameters [12]. The same relationships were also developed for basic recirculating buffers for comparison. The recirculating buffer simply has a constant index across the bit rate range. Therefore, dispersion places only a limit on the delay in number of bits. However, the maximum and minimum bit rates can be defined by the dispersion limit and practical size limit with several assumptions.

Fig. 4(a) plots the results of the study in [12] to demonstrate that bit rate greatly restricts both subsets of slow light approaches. Material-based resonator devices and coupled resonator structures are limited by linewidth and third-order dispersion as bit rate increases and by dephasing (loss) for low bit rates. It can also be seen that as the bit rate increases, the index of refraction decreases. The maximum bit rate is the point at which it is no longer possible to subject the data to the dispersive slowing phenomena without damaging the data. Integrated recirculating buffers implementing either silicon or silica delay lines are limited at low bit rates due to practical size considerations and are limited in length by second-order dispersion. Fig. 4(b) shows the effect of requiring operability for more reasonable packet lengths of 200 bits (25 bytes). Although this packet length is still not long enough for reasonable throughput, it is close to the maximum length that can be used with any slow light approach—only an ideal coupled resonator structure would be able to operate in this regime. The packet length defines the minimum required delay time to perform the buffering needed to resolve contention and therefore the minimum length of the device. As the device becomes longer, less dispersion is acceptable.

Feedback buffers are beneficial for their low component count and small footprint. Recirculating buffers meet all necessary requirements. Limitations resulting from noise accumulation can be reduced with optical filtering as performed in optical transmission systems. Although feedback buffers are optimized for a set packet length, solutions are being examined to manage this issue externally. Most importantly, the devices described here offer a solution that combines a compact footprint while allowing practical throughput. In addition, the feedback buffer is the only approach which can be easily configured to offer simultaneous reading and writing as well as speed-up. So in conclusion, as an overall solution, integrated recirculating buffers offer the most practical compromise.
3. INTEGRATED OPTICAL BUFFER FOR PACKET-SWITCHED NETWORKS

In this section, we demonstrate the first optical buffering of 40-byte packets of 40 Gb/s data using an on-chip optical buffer. The device consists of an InP-based, fast 2×2 switch and a silicon oxynitride waveguide delay. The buffer is flexible in implementation, but is demonstrated here in the recirculation configuration, thus offering longer storage times in a smaller footprint.

3.1 Device structure and design

A. Buffer approach

The chip-scale buffering device presented here has been designed to provide a prototype toward a fully integrated device that offers flexibility in implementation. Two material systems are used to achieve both large gain (InP-based) and high transparency (silica-based). The base buffer cell is comprised of a fast InP 2×2 switch with monolithic amplifiers to compensate for propagation and coupling losses from a silica waveguide delay line. This base cell can be cascaded to allow for simultaneous storage of more packets. The array may be used either as FIFO (first-in-first-out) memory, or can allow for packets to be re-ordered if prioritization is implemented. For the most common packet length of 40 bytes (acknowledgement packets in TCP/IP), the devices should be used in recirculating operation to minimize the number of cells needed. Longer packet lengths are limited in recirculating operation by the length of the delay line, but an array of cells can provide for feed-forward operation (Fig. 2(a)) and unlimited packet length. With the addition of second read and write ports, the buffer can also be used for speed-up. In this report the devices are used as recirculating buffers, both as single base cells and arrayed.

B. InP 2×2 switch

The 2×2 switching device affords negligible power penalty for a data rate of 40 Gb/s, the ability to switch within packet guard bands (<2 ns), high extinction ratios (>40 dB) for cascadability, and enough gain to compensate for its own insertion loss as well as that of the delay loop. A semiconductor optical amplifier (SOA) gate matrix is used as the switching structure to guarantee low crosstalk and for fast switching. Four gain amplifiers are monolithically integrated with the six switching amplifiers and are all less than 650 μm to reduce saturation effects. The schematic of the switch with the delay is shown in Fig. 5. Details of the switch operation and characterization were reported previously in [17].

![Fig. 5 Schematic of an SOA gate matrix switch with a delay.](image)

C. Silica recirculation loop

The recirculating loop is the other essential component of the buffer, important for providing nearly transparent delay. A silica-on-silicon buried ridge waveguide of core dimensions 5.5 × 5.5 μm² provided the necessary low propagation loss at the small expense of large bend radii. The index contrast using silicon oxynitride was 0.76%, standard for the foundry, ANDevices. The waveguide design is conservatively limited to a minimum bend radius of 6 mm, but was spiraled on the chip to reduce space. The area needed for 2 m of delay is 6.4 cm². Passive measurements were taken over a wavelength range from 1525 nm to 1575 nm for the silica waveguides to verify that long lengths of delay are possible. Measurements show propagation losses of less than 0.04 dB/cm at 1550 nm, varying less than 0.001 dB/cm over the 50 nm span. Polarization dependent loss for 200 cm of waveguide was approximately 1 dB and chromatic dispersion was approximately 130 ps/nm·km.

3.2 Results and discussion

A. Measurement setup

The InP devices were soldered and wirebonded to aluminum nitride submounts and cooled to approximately 20°C. The silica delay chip was held using a stage with 6 degrees of freedom to align the two pairs of waveguides simultaneously.
The optical signal (1560 nm) was modulated and analyzed using an SHF 50 Gb/s BERT with RZ 2^{31}-1 pseudo-random bit sequence (PRBS) data at 40 Gb/s. A variable attenuator and a polarization controller were placed in the setup before the device to maintain a TE-polarized input since the amplifiers are polarization dependent. A 1.2-nm bandpass filter was placed before the receiver to reduce the amplified spontaneous emission (ASE). Optical data packets at 40 Gb/s were generated to test multiple circulations. Layer 2 packet measurements used 40-byte packets that were analyzed with a PC as the BERT cannot synchronize with data that contains long blank spaces. The packet consists of a 32-bit idler, 64-bit identifier, 8-bit label, and 216 bits of repeated PRBS 2^{-1}. The label strings allowed for packet reordering and the identifiers were evaluated upon receipt for bit errors to determine if the packet was recovered. The switch timing was synchronized with the packet arrival using a payload envelope detect circuit and field programmable gate array (FPGA) based board.

**B. Device characterization**

The photonic chip buffer is comprised of the InP switch and silicon oxynitride waveguide delay and achieved 64 ns of packet storage (5 circulations). The total loop loss without gain is estimated to be 30 dB, composed of 8 dB of silica propagation loss, 14 dB for two couplings between the chips, and the remainder from the InP circuit losses. The four amplifiers in the path provide slightly more gain for one circulation, but the buildup of amplified spontaneous emission (ASE) lessens the gain for greater numbers of circulations. In order to find the optimal input power and the dynamic range of the buffer, the power penalty at a BER of 10^{-9} was measured for one circulation. Fig. 6(a) shows that the dynamic range was approximately 15 dB, thus making it practical for system use and allowing for multiple devices to be cascaded. Negative power penalty was observed due to the reduction of noise between packets from the gating SOAs as well as from slight pulse reshaping from the SOAs. Packet memory was then tested with the photonic chip buffer and 5 circulations (64 ns) was reached with 98% packet recovery (98% of packet identifier strings having no incorrect bits) (Fig. 6(b)).

![Fig. 6 (a) Dynamic range of input power for one circulation with 40 Gb/s RZ 2^{31}-1 PRBS. Insets show scope traces of the bit stream. (b) Packet recovery measurements showing 98% packet recovery for up to 5 circulations, or 64 ns of storage, using a silica delay chip.](image)

**C. System applications**

Some systems experiments have been performed to show the feasibility of this integrated buffer for contention resolution. Autonomous contention resolution was performed with 99% packet recovery for a packet capacity of 2, as well as for 2 separate buffered channels [18]. Furthermore synchronous optical packet buffering with this integrated buffer was demonstrated. Asynchronously arriving packets were optically synchronized to a local frame clock and loaded synchronously into the optical buffer. Packet recovery measurements of 40-Byte return-to-zero packets at 40 Gb/s showed error free performance [19].

**3.3 Conclusions**

The packet capacity and maximum storage time of this buffering approach can be increased to provide a realistic solution for optical routing. The optimization of the amplifier material platform and a decrease in loop losses are highly important. In order to lengthen the storage time the output saturation power of the amplifiers should be increased and, even more importantly, the noise figure should be decreased. The key to a low noise figure is a decreased internal loss, especially for amplifiers with small confinement factors. In addition, a decrease of 15 dB of total loop loss would result in increasing the maximum number of circulations from 5 to 25 for a noise figure of 6, assuming an OSNR of 20 dB is
required. This decrease in loop loss may be realized by reducing the coupling loss between the InP and silica waveguides using spot size converters. The first on-chip optical buffer for 40-byte packet lengths and a bit rate of 40 Gb/s demonstrated successful contention resolution between two packet streams. A single memory element showed up to 5 circulations, or 64 ns of storage, with 98% packet recovery. The results presented used the buffers in a recirculating configuration, but the buffer can also be used in feed-forward operation for longer packet lengths. These strengths show that optical buffering elements consisting of SOA-gated switches and silica waveguides offer a promising solution for populating buffers in optical routers. Multiple delay lines can be efficiently packed into the same size by interleaving waveguides in the same spiral. Consequently, up to 100 such buffers could be integrated onto a single die.

4. INTEGRATED HYBRID SILICON RECIRCULATING OPTICAL BUFFER

This section reports an integrated optical buffer consisting of a low loss silicon waveguide delay line and a hybrid silicon gate matrix switch. The integrated device demonstrates an error free operation at 40 Gb/s data rate with a packet delay of 1.1 ns. This demonstration also highlights the hybrid silicon platform to realize new types of photonic integrated devices by combining the low loss silicon passive components with the hybrid silicon photonic active devices.

4.1 Device structure and fabrication

Fig. 7(a) shows a layout of the integrated device. This is a recirculating optical buffer structure consisting of a silicon delay line and a gate matrix switch with additional boost amplifiers. Once optical packets are routed into the delay line, they are stored in the delay line until the gate matrix switch re-routes them to the output. The 2×2 gate matrix switch consists of two MMI splitters and four switching amplifiers. Input packets are split into two output ports and one of the split signals is gated by the amplifiers to a desired output port as illustrated in Fig. 7(b). Since this is based on a broadcast-and-selection method, there is an inherent loss of 6 dB from the input splitters and the output combiners. However this loss can be compensated from the optical gain of the switch amplifiers. The gate matrix switches are important for high cross talk suppression and high extinction ratio from the high absorption by reverse-biasing the amplifiers. However, the amplifiers need to be designed properly to ensure operation with a low power penalty from amplified spontaneous emission (ASE) noise.

Fig. 8 shows the process flow of the devices. After silicon waveguides are dry etched, a 0.5-μm thick SiO$_2$ layer is deposited on the silicon sample without removing a SiO$_2$ hard mask layer. Then, the silicon waveguide region for the amplifiers and the switch, where the III-V sample will be bonded, is exposed by wet-etching the SiO$_2$ layer by buffered HF. After a cleaning procedure, the III-V sample is roughly aligned by tweezers and bonded on the opened silicon region. The SiO$_2$ layer on the delay line region serves as a protection layer from scratches and any possible contaminations which can be caused by the bonding process. This will be further discussed in section 5.1. After anneal and InP substrate removal, the III-V layer for the amplifier and the switch is lithographically defined by a CH$_4$/H/Ar-based plasma reactive ion etch. An additional 0.5-μm thick SiO$_2$ layer is deposited for the protection of the silicon waveguides in the switch region. Then the III-V region is opened by CHF$_3$ based dry etching of the SiO$_2$ layer. Finally the amplifiers are fabricated on the exposed III-V region using the self aligned process described in [20]. The silicon waveguide in the delay line region is protected by ~ 1 μm thick SiO$_2$ layer. After all of the III-V processing is finished, ~ 0.7 μm thick SiO$_2$ layer still covers the silicon waveguides and is also used as a waveguide cladding. Fig. 9(a) shows
SEM images of the fabricated amplifiers in the optical buffer. The fabricated silicon waveguide has a width of 2 μm, a height of 0.7 μm, and a slab height of 0.4 μm. The total length of the silicon delay line is 9 cm. The minimum bend radius of the silicon delay line is 500 μm so that the bend loss is minimized. On a ~ 0.6×1 cm² chip, four devices are integrated by interleaving four delay lines. The fabricated device is mounted on an aluminum nitride (AlN) carrier and the electrical pads of the device are wire-bonded to the carrier for device probing using a probe card. An image of the mounted device is shown in Fig. 9(b).

4.2 Experiments and results

The device is mounted on a temperature controlled stage set to 15 °C. Lensed fibers are used for the input and output light coupling. The loss of a 9-cm long delay line is first measured to be 15 dB from a test structure which has the same waveguide design as the integrated device without the amplifiers and the couplers. The gain of the amplifier is characterized by measuring photocurrents from an adjacent reverse-biased amplifier. The input and output amplifiers are 1200 μm long while the switch amplifiers are 800 μm long. The maximum gain of the input/output and switch amplifier is 8 dB and 6 dB respectively. The ideal 3 dB loss of the MMI splitter is used to estimate the chip gain of the amplifiers. The available net gain from these amplifiers is enough to compensate the delay line loss of 15 dB.

The crosstalk and DC extinction ratio of the gate matrix switch is measured to be -34 dB and 30 dB respectively. The rise and fall times are slightly under 1 ns for an input power variation of -9 to -1 dBm. In general, the switching time is dependent on the electrical circuit response and the carrier lifetime of the amplifier [21]. The integrated device performance was evaluated with a return-to-zero (RZ) pseudorandom bit sequence (PRBS). Fig. 10 shows the test setup used for the measurements. A return-to-zero (RZ) 40 Gb/s data packet at a wavelength of 1560 nm was transmitted through a single mode fiber after amplification by an EDFA. An attenuator and a polarization controller are used between the transmitter and the device to control the input power and the polarization. The polarization is set to TE to
maximize the optical gain of the on-chip amplifiers in the device. The output signal of the device is amplified by an additional EDFA and then is received by a high speed receiver. The ASE noise of the input and output signal is filtered by band pass filters with 1.2 nm spectral band width. The power level to the receiver is controlled by a VOA to facilitate BER measurements at different receiver input powers.

![Fig. 10 Schematic diagram of the testing setup](image)

Fig. 10 Schematic diagram of the testing setup

Fig. 11 shows data packets (2^31-1) with two different switch configurations (through and cross-over). The figure shows a packet delay of 1.1 ns after one recirculation through the 9-cm long delay line (Fig. 11(b)). The additional insertion loss after one recirculation is 2.6 dB because the signal wavelength (1560 nm), which is chosen for EDFA amplifications, is different from the gain peak of the on-chip amplifiers (1572 nm). The plots on the right side of Fig. 11 show a close-in view of the received packets. The packet after one recirculation has slightly more power fluctuations due to the ASE noise from three additional on-chip amplifications.

![Fig. 11 (a). Data packet without recirculation (through switch state) (b) Delayed data packet after one recirculation (cross-over switch state).](image)

Fig. 11 (a). Data packet without recirculation (through switch state) (b) Delayed data packet after one recirculation (cross-over switch state).

To quantify the effect of the multiple amplifications, bit-error-rate (BER) measurements with 2^31-1 PRBS data streams were carried out. Fig. 12(a) shows the measured BER as a function of power at the receiver with different input power levels to the device. In general, BER of the delayed signal is higher than non-delayed signal as shown in the figure. Fig. 12(b) shows the power penalty at a BER of 10^-9 as a function of the input power. The power penalty without the delay is less than 1 dB with an input power variation of -16 to -4 dBm. However, the power penalty with one recirculation increases up to 4.3 dB because of additional ASE noise and shows a bathtub curve minimized at an input power around -10 dBm. At a low input power, the power penalty is dominated by the ASE noise while at a high input power the power penalty increases again because of the saturation of the amplifiers. The input dynamic range for less than a 3 dB power penalty is 8.5 dB for one recirculation.

In order to understand the current device performance, a simple device model, shown in Fig. 13, is analyzed. The model is based on a cascaded amplifier link consisting of lossy passive components and amplifiers. In this model, only the effect of the ASE noise is considered to simplify the problem.
The signal transmission in the device can be divided into three stages: 1) input stage, 2) recirculating stage, and 3) output stage. The effect of transmission through each stage is represented by an effective noise factor and a net gain, which can be calculated using a simple model of a cascaded chain of passive elements and amplifiers [22]. The detailed mathematical derivation is omitted here, and the resulting net noise figure of each stage is shown in Fig. 13. From the noise factor and the net gain of each stage, the effective noise factor of the entire device can be derived as a function of a number of recirculation (N), which is written as:

\[ F_{\text{net}}^{\text{N=0}} = F_{\text{IN}} + \frac{F_{\text{OUT}}}{G_{\text{IN}}} \] , for 0 circulation, \hspace{1cm} (1a)

\[ F_{\text{net}}^{\text{N>0}} = F_{\text{IN}} + \frac{F_{\text{LOOP}}}{G_{\text{IN}}} \sum_{k=1}^{N} \frac{1}{G_{\text{LOOP}}^{k-1}} + \frac{F_{\text{OUT}}}{G_{\text{IN}} G_{\text{LOOP}}^{N}} \] , for N circulations. \hspace{1cm} (1b)

Since the device needs to be biased below the lasing threshold, there is another constraint that the net gain of the recirculating stage \((G_{\text{LOOP}})\) should be less than unity. Applying this condition to Eq. (1), the minimum noise factor after \(N\) recirculations occurs when \(G_{\text{LOOP}}\) is unity and is written as:

\[ F_{\text{net}}^{\text{N>0}} = F_{\text{IN}} + \frac{F_{\text{LOOP}}}{G_{\text{IN}}} N + \frac{F_{\text{OUT}}}{G_{\text{IN}}} \] , for \(G_{\text{LOOP}} = 1\). \hspace{1cm} (2)

**Fig. 13** Device model using a cascaded link of the passive elements and the amplifiers. In this diagram is \(G_{i}\) the gain of the input amplifier, \(G_{\text{sw}}\) the gain of the switch amplifier, \(G_{j}\) the gain of the amplifier in the loop, \(L_{\text{MMI}}\) the MMI transmission (-3dB), \(L_{\text{loss}}\) the loop loss and \(F\) the noise figure of the amplifier (assumed to be 7 dB [23]).

Eq. (2) suggests several ways to minimize the signal degradation from the ASE noise accumulation. First, the noise factor increases linearly as the number of the recirculations increases with a rate of \(F_{\text{LOOP}}/G_{\text{IN}}\) which is de-emphasized noise factor by the input amplifier gain at the recirculating stage. Therefore the input amplifier gain \((G_{\text{IN}})\) needs to be high enough to suppress the effect of the noise accumulation from the multiple recirculations. Next, the noise factor of the recirculating stage \((F_{\text{LOOP}})\) needs to be minimized for the same reason. As shown in the equation in Fig. 13, \(F_{\text{LOOP}}\) is
primarily determined by a product of the loop loss and the gain of the loop amplifier \((G_d \cdot L_d)\), which implies that signal power entering the loop needs to be pre-amplified with a higher gain. The power penalty can be estimated by calculating receiver sensitivity for each recirculation. To simplify the calculation, it is assumed that ASE noise is dominant on the receiver sensitivity over other factors such as modulation format and timing jitter. Eq. (3) is used for this calculation and the power penalty is defined as receiver sensitivity degradation at a BER of \(10^{-9}\). A -27-dBm receiver sensitivity, which is estimated from the back-to-back BER measurements, is used as a reference. This equation also makes the approximation that the shot and thermal noise are negligible compared to the beat noise of the ASE against itself and the signal [24].

\[
P_{\text{rec}} = h \nu F_{\text{max}}^\text{mat} \left( Q^2 + Q \left( \frac{\Delta \nu_{\text{opt}}}{\Delta f} \right)^{0.5} \right)
\]

where \(h\), \(\nu\), \(\Delta f\), \(\Delta \nu\), and \(Q\) are Planck’s constant, optical frequency, electrical bandwidth of the receiver, optical bandwidth of the bandpass filter, and quality factor, respectively.

Fig. 14 shows the calculated power penalty as a function of a number of recirculation with a different loss of the delay line and gain of the input amplifier. A quality factor (Q) of 6 is used which corresponds to a BER of \(10^{-9}\). The optical and electrical bandwidth are assumed to be 2 nm (246 GHz) and 40 GHz respectively. As shown in the figure, the input amplifier gain and loop loss are crucial factors affecting the quality of the signal after many recirculations. With a lower loop loss and higher input amplifier gain, the effect of the noise accumulation can be suppressed further. It is predicted that 9~10 recirculations with a power penalty of 2 dB can be achieved if a loop loss and an input amplifier gain can be 15 dB and 10 dB, respectively. However it is inevitable to have a more loss from a longer delay line. A delay of 10 ns corresponds to a ~80 cm long silicon waveguide resulting in a typical loss of 20 ~30 dB even with a sub-dB/cm waveguide loss. Therefore, adding one or two more amplifiers inside the delay line will lead to better performance in this case. Signal degradation from the pattern effects needs to be considered and weighted with the benefits from additional amplifications. In addition, the device layout has to be laid out carefully in order to suppress thermal run-away effect due to the integration of many optical amplifiers.

### 4.3 Conclusions

An integrated optical buffer operating at 40 Gb/s is demonstrated in this section. The device consists of the silicon delay line and the gate matrix switch built on the hybrid silicon platform. The silicon delay lines are designed to minimize the bend loss, yet they are still compact enough to enable the entire device to be laid out within a 0.6×1 cm² space. The gate matrix switch is chosen over other types of optical switches because of a low cross talk of -30 to -40 dB. The fabricated device demonstrates a 1.1-ns delay of 40 Gb/s data packets. The minimum power penalty with a 1.1-ns delay is 2.5 dB with an input dynamic range of 9 dB. Further improvements on the waveguide loss and the amplifier gain should improve the device performance, leading to a longer buffering time, and will provide enough functionality as integrated optical buffers for all optical packet switched networks. In addition, this structure can be directly extended to integrated optical synchronizers with several gate amplifiers [25].
5. 40-BYTE BUFFERS ON THE HYBRID SILICON PLATFORM

This section summarizes our current efforts to realize a fully integrated recirculating optical buffer on the silicon evanescent device platform, capable of storing 40-byte packages, i.e. having a delay line of 1.1 m. In section 4 we have successfully demonstrated a fully integrated buffer with a delay line of 9 cm, corresponding to a delay of 1.1 ns. The device performance was limited by the delay line losses, which were in the order of 1.8 dB/cm. In this section we present an overview of our efforts to reduce the silicon waveguide loss. Although these losses can be compensated by optical amplifiers placed at regular spaces along the delay line, these amplifiers will decrease the signal-to-noise ratio by adding noise in the form of amplified spontaneous emission to the signal.

5.1 Silicon waveguide loss optimization

Since the fully integrated optical buffer consists of a silicon waveguide delay, low propagation losses and the reduction thereof are of the utmost importance. We measured typical loss values for 2-μm wide, 0.7-μm high rib waveguides (~50% etch depth) of 0.8 dB/cm after the silicon etch, increasing up to 1.8 dB/cm after the III/V bonding and consecutive processing, as shown in Fig. 8. For a delay line of 1.1 m length, these loss values would add up to around 200 dB delay line loss. Hence it is clear that the waveguide losses have to be reduced significantly.

A. Silicon waveguide fabrication

The silicon waveguide fabrication process contributes about 0.8 dB/cm to the total buffer loss, which is about 0.5 dB/cm higher than state-of-the-art. Loss contributions can be divided into material losses and waveguide losses, e.g. due to sidewall roughness. The material losses were minimized by having a special undoped epitaxial silicon growth on top of the SOI wafer. The waveguide roughness is typically caused by lithographic and etch contributions. By optimizing the photoresist baking conditions (see Fig. 15), we were able to reduce our waveguide losses from 0.8 to 0.66 dB/cm average and 0.5 dB/cm best-case. There is an ongoing effort to decrease this value further by optimizing the waveguide etch conditions.

B. Additional waveguide losses due to III/V processing

The (passive) silicon waveguide loss of a fully fabricated buffer is higher than the loss right before banding to the III/V and consecutive processing. The loss increases from 0.8 to 1.8 dB/cm. There is strong evidence that the increase in loss is due to impurities (primarily Sodium, see Fig. 16) that diffuse through the SiO₂ layer that protects the waveguide while the active regions on the chip are processed. While the Sodium ions do not reach the waveguides, they attract free electrons in the waveguide. This leads to free carrier absorption, and contributes to the loss. Even a thick SiO₂ layer does not prevent the Sodium from diffusing through the top SiO₂ layer. Currently we have implemented a SiN layer in the protection layer which acts as a Sodium diffusion blocking layer. Another possible reason for the increased losses can be structural damage to the silicon rib waveguides due to stress and/or strain in the oxide layer covering the passive waveguides.

5.2 Conclusion and outlook

It has been shown previously that optical buffers present a realistic solution for solving network contention [13]. However these buffers must meet certain requirements to achieve acceptance. In this paper we show that optical buffers in a recirculating, or feedback, configuration are able to meet all requirements for 40-Gb/s operation with reasonable packet payload lengths. This is unlike alternative approaches based on slow light, where bitrate is limited by operating
bandwidth of the element and packet length is limited to about 200 bit operation in the most ideal case of a perfect coupled resonator structure. Only a recirculating buffer approach is able to store packets of at least 40 bytes, which is required for feasible contention resolution.

Feedback buffers are beneficial for their low component count and small footprint. Limitations resulting from noise accumulation can be reduced with optical filtering. Integration on an optical chip of these buffers is attractive for reasons of cost, robustness and potential mass fabrication. Silicon and silica delay lines are possible candidates to create low-loss delay lines, used in the buffer. In this paper we have presented the first on-chip optical buffer capable of buffering 40-byte packets of 40 Gb/s. The device consists of an InP-based, fast 2×2 switch and a silicon oxynitride waveguide delay. This shows the feasibility of integrated optical buffers to be used in an optical network.

To ease packaging and alignment requirements and consequently costs a single-chip approach is most favorable. We have presented in this work the first fully integrated optical buffer, fabricated in the hybrid silicon platform. The buffer has a delay of 1.1 ns, limited by the silicon delay line losses. We have shown that the silicon delay line losses can in principle be significantly reduced, allowing for larger delay lines and scaling up to 40-byte operation. So concluding it can be stated that hybrid silicon integrated recirculating optical buffers are a promising approach for compact and scalable components that can operate at high data bit rates. As such they offer a feasible and flexible solution for future network contention resolution.

Fig. 16 Sodium concentration profile as a function of the depth as measured by SIMS. The 0.7-μm silicon waveguide (right-hand side) is covered by a 3.6-μm thick oxide layer.

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