Technologies and Systems of Optical Switching

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Abstract: We report on the latest advances in photonic technologies of functions required for optical routing and switching systems including wavelength conversion, monolithic tunable optical routers, payload envelope detection, packet forwarding, optical buffers, optical synchronizers, optical clock recovery, mode-locked lasers and 3R regeneration.

Keywords: Photonic integration, optical packet switching.

1. Introduction

The increasing demand for optical bandwidth and capacity of commercial electrical routers has pushed the power dissipation limits of today’s largely electronic based router designs and ignited new interest in the role optoelectronic and photonic technologies can play in decreasing power requirements. New thought is being given to router and network design to incorporate approaches that blend electronic and optical handling of packets in WDM fiber based networks. However, photonic and optoelectronic solutions must meet the economic and footprint demands that electronics has to offer. Photonic integration of these new functions is key to achieving this goal. The power consumption problem for today’s routers is partly due to the power spreading problem induced from increasing per chip power dissipation and the move to inter-chip, inter-linecard and inter-rack solutions with the overhead of optical interconnects and OEO interfaces as illustrated Figure 1.

Figure 1: Illustration of the power-spreading problem for high capacity electronic chip based routers

2. The LASOR Architecture

The LASOR optical data router (ODR) [1] [2] is shown in Figure 1. A network of LASOR nodes in a DODN network that is connected at the edge to legacy IP and other networks is shown in Figure 2. The LASOR optical data node (ODR) resides on a linecard in a node called an optical routing node (ORN). The ORN is a shelf system with WDM fiber input and outputs that are connect via a slowly reconfigurable backplane (ROB) to optical packet routing linecards for packet switching between node input and output ports, packet express through the linecard with wavelength conversion, or line rate add/drop to the local node. This combination of packet switching, circuit switching and express bypass leads to a highly scalable design with the potential for high throughputs with low power consumption and small footprint. We are targeting a linecard capacity of 5Tbps.

Figure 2: A network of LASOR ORNs and ODRs.

A simple example of a 4-input, 4-output LASOR ODR is shown in Figure 3. The key elements for each input are shown here and described in further detail later in this paper and in referenced publications. The two key paths are the all-optical payload path that contains a photonic integrated circuit (PIC) packet synchronizer, a PIC optical random access packet memory (ORAM) and a PIC packet forwarding chip (PFC). In parallel with this PIC based packet path is an optical label processing and PIC control path including the payload envelope detect (PED), the burst mode optical clock and data recovery (OCDR) and the forwarding and lookup electronics. An AWGR is used to direct packets on a per packet basis to the required output port after input buffering and a final stage of 3R regenerative wavelength converters retimes the payload bits and converts the payloads to the required outbound transmission wavelength.

Figure 3: LASOR Optical Data Router (ODR) Linecard Architecture.
The wavelength grid that LASOR operates on is designed to facilitate connection to arbitrary input and output WDM wavelength plans, optimize the performance of internal ODR components, to separate the switching and transmission functions and to allow fast switching without closed loop wavelength lockers. The switching plan transition in an ODR is illustrated in Figure 4.

### Table 1. Summary of LASOR ODR Functions, Integration Platforms, Performance and Publication References.

<table>
<thead>
<tr>
<th>Function</th>
<th>Integration Platform(s)</th>
<th>Performance Summary</th>
<th>Refs</th>
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<tr>
<td>Monolithic Tunable Optical Router</td>
<td>InP</td>
<td>640 Gbps routing capacity, 8 inputs 8 outputs, 40Gbps per input, 3R regenerative, C-band tunable</td>
<td>[18]</td>
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<tr>
<td>Optical Payload Envelope Detection</td>
<td>InP, Si/InP</td>
<td>40 Gbps variable length, asynchronous payloads, C-Band operation. 30ps recovered payload envelope rise time and 3ps rms jitter over 10dB dynamic input power range.</td>
<td>[3][4][5]</td>
</tr>
<tr>
<td>Optical Packet Synchronizer</td>
<td>InP/Silica, Si/InP</td>
<td>4-stage synchronizer with the relative delay through any configuration of the synchronizer given as $T(n) = n \times \Delta (n = 0, 1, 2 \ldots 15)$, where $\Delta = 800$ps and the tuning range is 12.8ns. Packet rate reconfiguration.</td>
<td>[6]</td>
</tr>
<tr>
<td>Burst Mode CDR</td>
<td>InP and Si Electronics</td>
<td>10Gbps asynchronous labels. &lt; 20 bit lock time and &gt; 380 bit hold time. BER $&lt; 10^{-12}$ and 0% header loss over 0.4dB Dynamic Range at input.</td>
<td>[7][8][9]</td>
</tr>
<tr>
<td>Optical Random Access Memory (ORAM)</td>
<td>InP/Silica, Si/InP</td>
<td>2.3ms delay, 40GbE in, &lt; 1ms load/unload switch times, 184ns storage of 40Byte 40GbE packets with &gt; 98% packet recovery after storage.</td>
<td>[10][11][12]</td>
</tr>
<tr>
<td>Packet Forwarding Chip (PFC)</td>
<td>InP</td>
<td>40Gbps asynchronous, variable length payload fast switchable wavelength conversion and 10Gbps optical label re-write. C-Band operation. -27dBm sensitivity, &lt;2dB PP.</td>
<td>[13][14][15]</td>
</tr>
</tbody>
</table>

The wavelength grid that LASOR operates on facilitates connection to arbitrary input and output WDM wavelength plans, optimizing the performance of internal ODR components, separating switching and transmission functions, and allowing fast switching without closed loop wavelength lockers. The switching plan transition in an ODR is illustrated in Figure 4.

3. Overview of PIC Integrated Technologies

The ODR functions have been integrated to the chip level using various PIC platforms. These PICS and performance highlights are summarized in Table 1 and described in further detail below.

#### 2.1 The Optical Payload Envelope Detector (PED)

The PED outputs to the electronic processing layer a temporally accurate envelope that stamps the location and duration of the payload in the optical domain in order to process functions like label erase and rewrite without recovering 40Gbps data.

#### 2.2 The Optical Packet Synchronizer (OPS)

The synchronizer is based on a feed-forward design that utilizes SOAs and optical delay lines as depicted in Figure 5. We have demonstrated a four stage synchronizer with the relative delay through any configuration of the synchronizer given as $T(n) = n \times \Delta (n = 0, 1, 2 \ldots 15)$, where $\Delta = 800$ps and the tuning range is 12.8ns.

- **Figure 4**: LASOR ODR wavelength plan from input to output.
- **Figure 5**: Schematics and picture of integrated packet synchronizer.
2.3 Optical Random Access Memory (ORAM)

The most successful optical buffering demonstrations have used either feedback or feed-forward buffers, many of which implement two-by-two or one-by-two switches [10][11][12]. Integrated solutions have only recently been demonstrated. A simple 450 centimeters (23 ns) re-circulating buffer based on an InP SOA gate array two-by-two switch and an optical fiber delay loop was reported (Figure 6). Greater than 40 dB extinction, sub-nanosecond switching, and fiber-to-fiber gain was demonstrated. Up to 184 ns of storage was shown with greater than 98% packet recovery for 40 Gb/s, 40-byte packets.

2.4 Optical Packet Forwarding Chip (PFC)

Packet forwarding in an optical router is performed through fast wavelength tuning, wavelength conversion of the payload, and encoding of a label for the outgoing packet. The PFC provides rapidly switched widely tunable wavelength converter with optical label re-write and 2R regeneration. The monolithically integrated wavelength converters contained within the PFC utilizes non-linear effects in a semiconductor optical amplifier (SOA) caused by the pump-probe signal interaction [13][15]. Wavelength conversion with both device types at bit rates of 40 Gbps RZ has been reported. Multistage tunable wavelength converter MZI-SOA based implementations with on chip signal filtering have been demonstrated as well [14].

2.5 The Optical Packet 3R Regenerator: Optical Clock Recovery and Mode Locked Lasers

Regenerators for optical data signals are essential components for long distance communication systems and signal regeneration with retiming, reshaping, and reamplification (3R) is periodically required. We have demonstrated a hybrid silicon evanescent ring mode-locked laser and evaluate its performance as an all-optical clock recovery element. The device, shown in Figure 7, is capable of generating a reshaped and retimed clock signal from 30.4 Gb/s data, even when the input data is severely degraded. For input data with 3.8 dB extinction ratio (ER) and 14 ps of jitter, the recovered clock has an ER over 10 dB and 1.7 ps of jitter.

2.6 Monolithic Tunable Optical Router (MOTOR)

We have demonstrated the first InP monolithic tunable optical router (MOTOR) with 8 input and 8 output ports and error-free 40 Gbps operation per port [18]. The resulting 640 Gbps capacity switch consists of eight wavelength-tunable differential Mach-Zehnder SOA wavelength converters with preamplifiers and a passive 8x8 arrayed-waveguide grating router as shown in Figure 8. Each wavelength converter employs a widely-tunable sampled-grating DBR laser for efficient wavelength switching across the C band and other functions required for differential 40Gbps wavelength conversion. Active and passive regions of the chip are defined through a robust quantum well intermixing process to optimize the passive loss in the AWGR and gain in the wavelength converters. The overall device is one of the most complex photonic ICs reported to date, with dimensions of 4.25 mm x 14.5 mm and more than 200 functional elements integrated on-chip. Using 231-1 PRBS data, a power penalty as low as 4.3 dB was achieved with less than 2 W drive power per channel and 16W power for the complete chip.

3. Acknowledgements

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5. References


