A Real-Time Asynchronous Dynamically Re-Sizable Optical Buffer for Variable Length 40Gbps Optical Packets


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Abstract: We demonstrate a 40Gbps dynamically re-sizable optical buffer capable of storing packets of lengths ranging from 40 to 800 bytes. Packet recovery measurements greater than 95% demonstrate a dynamic operating range of 5dB.

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1. Introduction

All-optical packet routers are being investigated to mitigate the challenges that all-electronic router designs are facing [1]. Optical packet buffering is one important approach to contention resolution and blocking in an optical router [2]. However, to date, optical packet buffer solutions depend heavily on re-circulating loop configurations that must be designed to accommodate the largest packet size with latency tradeoffs for the smallest packet sizes. Current IP networks consist of average packet sizes that vary from 40 bytes (40%) to 1500 bytes (10%) [3]. The majority of work in this field has provided several novel synchronous designs with theoretic analysis at data rates of 10Gbps [6-8]. We demonstrate for the first time a truly asynchronous, real-time, dynamically re-sizable optical buffer that adjusts its storage time based on the length of the packet to be stored. With this type of packet buffer variable or fixed length packets can be stored with the capability to know where the packet is in the loop at all times and to synchronize all variable length packet buffers using techniques that have been reported previously [4].

The re-sizable optical buffer is based on a digitally programmable delay line matrix within an integrated semiconductor optical amplifier (SOA) based re-circulating buffer. A payload envelope detection (PED) technique in combination with electronic lookup is utilized for buffer re-sizing [5]. The demonstration uses integrated optic technology and is amenable to implementation of the complete design at the chip level. The focus of this paper is on the implementation and experimental results of a dynamically re-sizable optical buffer for variable length 40Gbps optical packets.

2. Re-Sizable Optical Buffer Design

The challenge of a re-sizable optical buffer lies in the tradeoff between a compact design and flexibility. Larger packet lengths will require longer lengths of fiber delay in addition to several different lengths of fiber to provide an acceptable amount of packet length resolution. One could use a single length of fiber to accommodate the longest possible packet length that will effectively accommodate subjacent lengths, however, such a configuration may result in a diminished buffer throughput. Also, an effort must be made to compensate for the losses of the different fiber lengths while limiting the accumulation of amplified spontaneous emission (ASE) for each circulation.

Fig. 1(a) Re-circulating buffer with 2x2 InP switches (top) and re-sizable loop comprised of feed-forward stages (bottom).

(b) Re-sizable optical buffer experimental setup
The re-sizable optical buffer depicted in Fig. 1(a) uses a 2x2 InP offset quantum well SOA switch matrix to switch packets into and out of a variable length storage loop consisting of a 4-stage feed-forward switched delay. During operation, an input signal is gated either through the output port or towards the loop delay. Re-circulations are achieved by gating loop signals back towards the loop delay. The optical buffer has been shown to perform at bit-rates up to 40Gbps and meets the requirements of having low cross-talk (<-40dB), high extinction ratios (>40dB), and fast switching times (<2ns) [9]. The re-sizing function is carried out by inserting a four-stage feed-forward synchronizer, depicted in Fig. 1(a), within the buffer fiber loop. An optical band pass filter is inserted after the synchronizer to reduce the accumulation of ASE caused by the SOAs while a variable attenuator (VA) is used to equalize the power between buffered and non-buffered packets.

Each stage of the synchronizer consists of a pass arm in addition to a delay arm with a \( \Delta \)-delay that increases by powers of two at each stage [10]. The SOAs serve as on/off switches for the packets as well as a means for loss compensation. Isolators (ISO) are included to eliminate back-reflections, while VAs are used to match the power through any path combination within 1dB. Such a configuration results in delays of \( T_{n\Delta} = T_{0\Delta} + n \times \Delta \), where \( T_{0\Delta} \) and \( \Delta \) have been measured to be 232.47ns and 6.09ns respectively. Thus, the shortest path through the synchronizer is \( T_{0\Delta} = 232.47 \text{ns} \) while the longest path is \( T_{15\Delta} = 323.82 \text{ns} \). Layer-1 performance of the synchronizer was determined via bit error rate (BER) measurements for a range of input powers using a 40Gbps non-return to zero (NRZ) 2\(^{7}-1\) pseudo random binary sequence (PRBS). Fig. 2(a) shows the BER measurements at an input power of 5dBm for \( n \) values of 0, 5, 10, and 15. Fig. 2(b) depicts the power penalty measurements that were taken for an expected BER of 10\(^{-9}\). The degradation of the optical signal to noise ratio (OSNR) limits the synchronizer to a dynamic power range of 3dB of decreased power at less than 2dB power penalty.

Similar forms of payload envelope detection have been achieved using a photo-detector followed by a bandwidth-limited amplifier [5]. The relatively low duty cycle of the packet stream causes the signal to noise ratio (SNR) of the amplifier to deteriorate significantly. An all-optical payload envelope detector (AO PED) circuit, that consists of two stages of cross-gain modulated (XGM) SOAs, is used as an alternative in order to reduce rise and time fall times in addition to timing jitter of low duty cycle signals [11]. The rise time of the PEDs was 350ps.

### 3. Experimental Results

A diagram of the re-sizable buffering is shown in Fig. 1(b). A bit pattern generator (BPG) is used to modulate a 1560nm CW signal at 40Gbps that is split into a data path and a PED path. The PED path is forwarded to the AO PED circuit that generates PED signals that are sampled by the buffer controller (BC) to establish the location and the length of each amplifier. The electronic lookup table used by the BC to re-size the optical buffer is shown in Fig. 2(c). A processing delay (\( T_{\text{proc}} = 190\text{ns} \)) is included in the data path to account for the finite processing time of the BC which includes the time required for PED generation. The BC consists of a field programmable gate array (FPGA) based controller that generates the required buffer and synchronizer SOA signals. Buffered packets are then sent to an optical receiver for packet recovery measurements. The BC doubles as a second optical transmitter used to inject dummy packets into the packet stream for the sole purpose of increasing packet stream duty cycle to facilitate data recovery.

The maximum allowable buffer size is limited by the longest path through the synchronizer (\( T_{15\Delta} = 323.82 \text{ns} \)). The buffer fiber delay was chosen to be twice the temporal length of the packet to allow for less stringent contention resolution requirements. Packet sizes of 40, 400, 600, 650, 700, 750, and 800 bytes were chosen to test the ability of the buffer to be re-sized. Each packet consists of the following structure: 32-bit idler, 64-bit unique packet identifier and a repeating 2\(^{7}-1\) PRBS pattern.
Different buffer sizes will require asynchronous burst-mode clock and data recovery which is difficult to perform at 40Gbps. As a result, synchronous packet recovery measurements were performed on streams of 40Gbps NRZ packets of a single length of delay. The amount of space between packets was determined by the BC processing time \( T_{\text{proc}} \) and the time required for the maximum amount of circulations \( 3 \times T_{\text{155}} \) that resulted in stream duty cycles of 9% and 0.5% for 800- and 40-byte packet streams respectively. Additionally, the BC was programmed to buffer all incoming packets in order to study the performance of buffer re-circulations.

Packet recovery curves, performed on \( 1/4 \) of 40Gbps packet identifiers, for packets lengths of 40 bytes and 800 bytes are shown in Fig. 3(a) and (b) respectively. The 800-byte stream can be circulated up to two times with a packet recovery greater than 95% over a 5dB dynamic range. On the other hand, the 40-byte stream is only capable of achieving up to one circulation over a 4dB dynamic range. The optical buffer in question has been demonstrated to achieve up to eight circulations, in fixed length experiments, limited by the accumulation of ASE [9]. The current buffer configuration further exacerbates the ASE buildup since packets must pass through four additional SOAs per revolution. The discrepancy in packet recovery between the two streams can be explained by difference in optical signal to noise OSNR of the two streams caused by the differing stream duty cycles.

4. Conclusion

An implementation of a dynamically resized optical buffer is demonstrated using 40Gbps NRZ optical packets of sizes ranging from 40 bytes to 800 bytes. Up to two circulations in the best (800 bytes) and one circulation in the worst (40 bytes) cases are achieved with packet recovery greater than 95% over a dynamic power range of 5dB.

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5. References